NCP5214

Product Preview

2-in-1 Notebook DDR Power Controller

The NCP5214 2−in−1 Notebook DDR Power Controller is specifically designed as a total power solution for notebook DDR memory system. This IC combines the efficiency of a PWM controller for the VDDQ supply with the simplicity of linear regulators for the VTT termination voltage and the buffered low noise reference. This IC contains a synchronous PWM buck controller for driving two external NFETs to form the DDR memory supply voltage (VDDQ). The DDR memory termination regulator output voltage (VTT) and the buffered VREF are internally set to track at the half of VDDQ. An internal power good voltage monitor tracks VDDQ output and notifies the user whether the VDDQ output is within target range. Protective features include soft−start circuitries, undervoltage monitoring of supply voltage, VDDQ overcurrent protection, VDDQ overvoltage and undervoltage protections, and thermal shutdown. The IC is packaged in DFN−22.

Features

- Incorporates VDDQ, VTT Regulator, Buffered VREF
- Adjustable VDDQ Output
- VTT and VREF Track VDDQ/2
- Operates from Single 5.0 V Supply
- Supports VDDQ Conversion Rails from 5.0 V to 24 V
- Power−saving Mode for High Efficiency at Light Load
- Integrated Power FETs with VTT Regulator Sourcing/Sinking 1.5 A DC and 2.4 A Peak Current
- Buffered Low Noise 15 mA VREF Output
- All External Power MOSFETs are N−channel
- <5.0 μA Current Consumption During Shutdown
- Fixed Switching Frequency of 400 kHz
- Soft−start Protection for VDDQ and VTT
- Undervoltage Monitor of Supply Voltage
- Overvoltage Protection and Undervoltage Protection for VDDQ
- Short−circuit Protection for VDDQ and VTT
- Thermal Shutdown
- Housed in DFN−22

Typical Applications

- Notebook DDR/DDR2 Memory Supply and Termination Voltage
- Active Termination Busses (SSTL−18, SSTL−2, SSTL−3)

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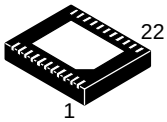
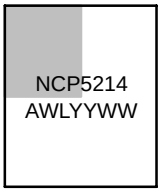
MARKING DIAGRAM

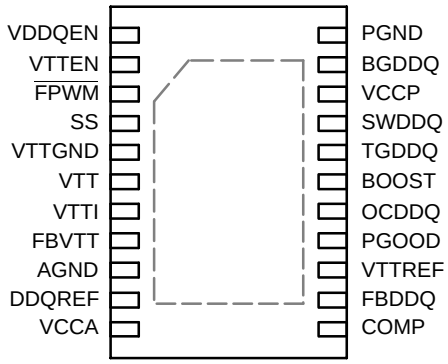


DFN−22
MN SUFFIX
CASE 506AF



NCP5214 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



(Top View)

NOTE: Pin 23 is the thermal pad on the bottom of the device.

ORDERING INFORMATION

Device	Package	Shipping†
NCP5214MNR2	DFN−22	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

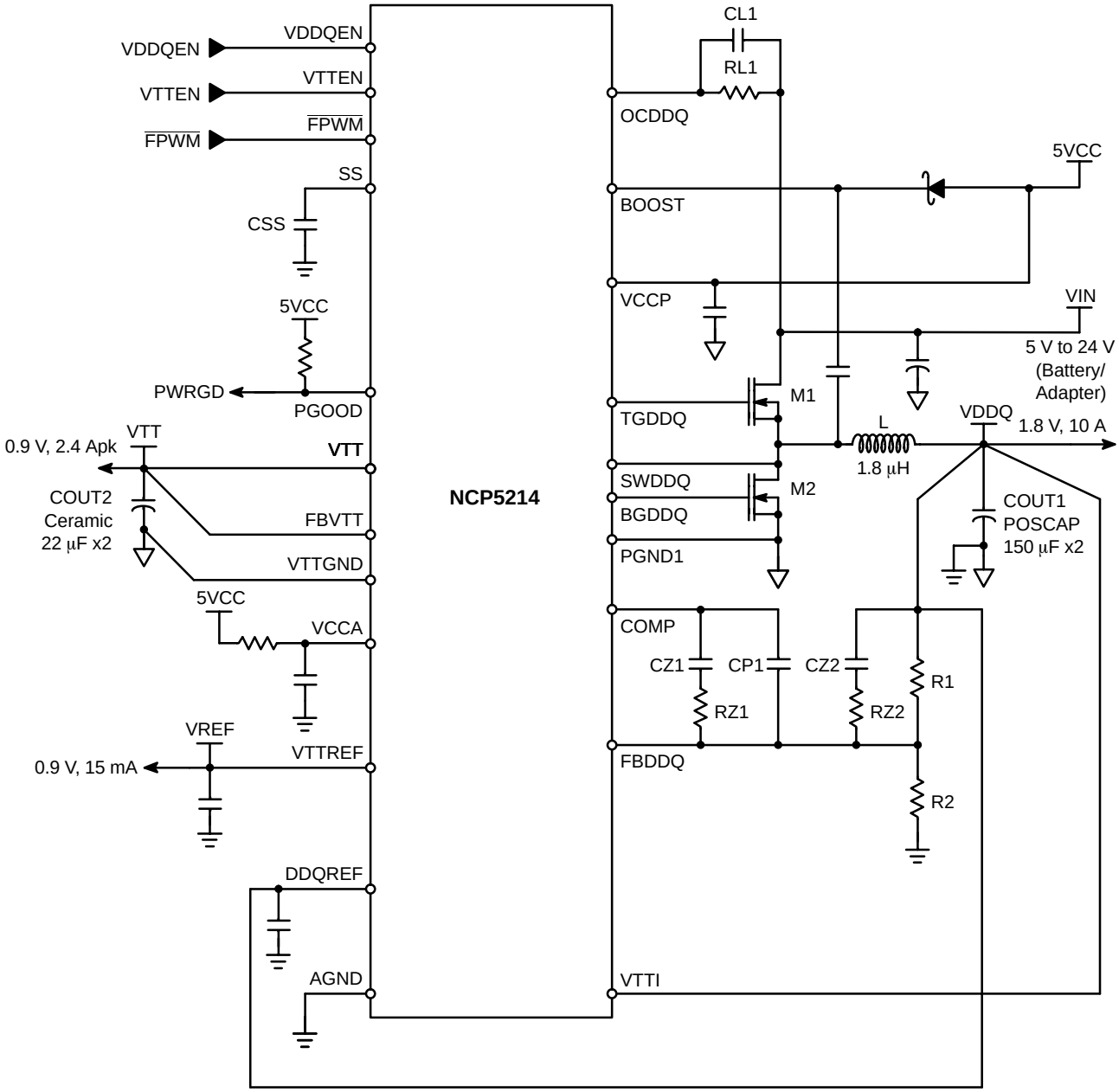


Figure 1. Typical Application Diagram

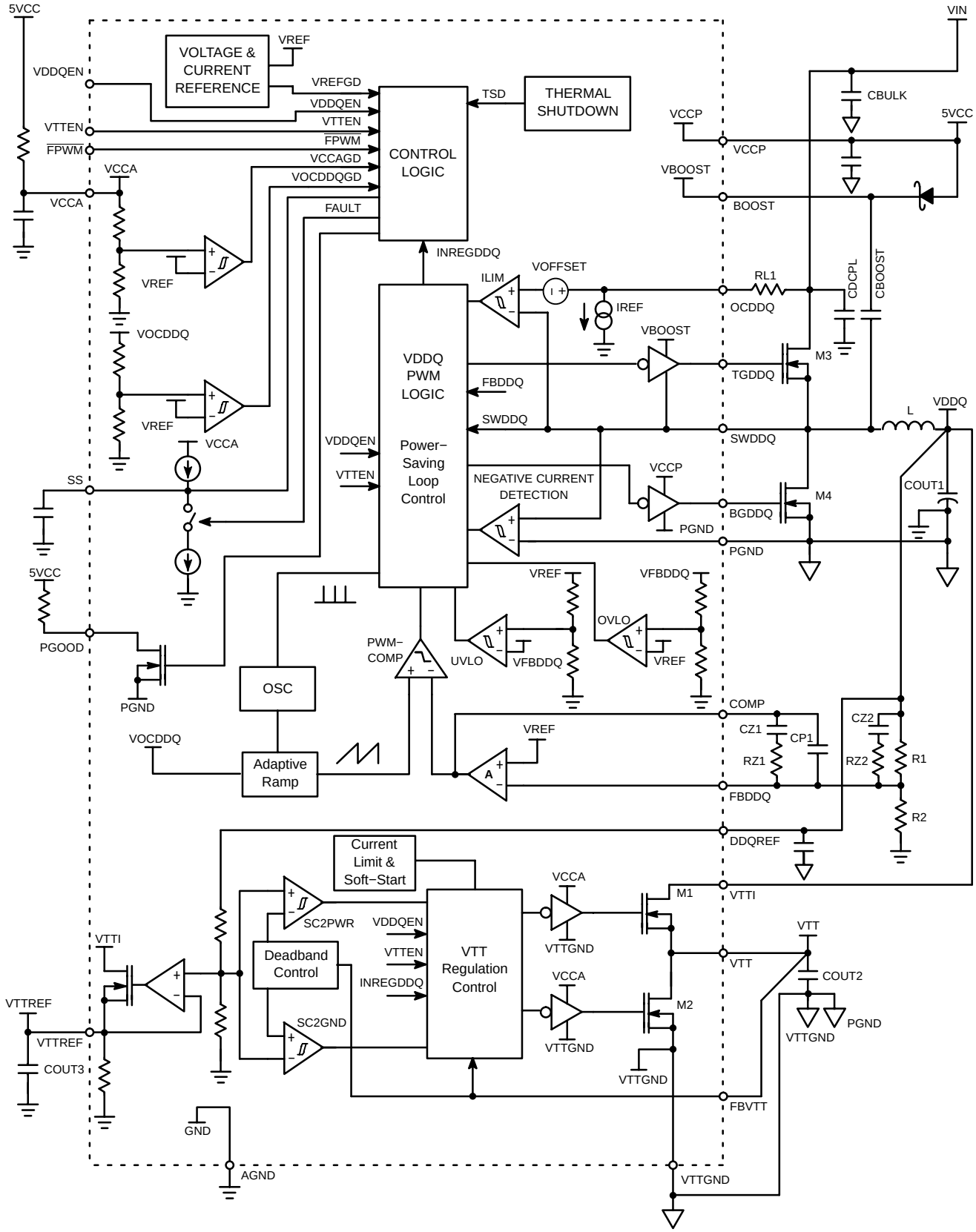


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	VDDQEN	VDDQ regulator enable input. High to enable.
2	VTTEN	VTT regulator enable input. High to enable.
3	$\overline{\text{FPWM}}$	Forced PWM enable input. Low to enable forced PWM mode and disable power−saving mode.
4	SS	VDDQ Soft−start capacitor connection to ground.
5	VTTGND	Power ground for the VTT regulator.
6	VTT	VTT regulator output.
7	VTTI	Power input for VTT regulator which is normally connected to the VDDQ output of the buck regulator.
8	FBVTT	VTT regulator feedback pin for closed loop regulation.
9	AGND	Analog ground connection and remote ground sense.
10	DDQREF	External reference input which is used to regulate VTT and VTTREF to 1/2VDDQREF.
11	VCCA	5.0 V supply input for the IC's control and logic section, which is monitored by undervoltage lock out circuitry.
12	COMP	VDDQ error amplifier compensation node.
13	FBDDQ	VDDQ regulator feedback pin for closed loop regulation.
14	VTTREF	DDR reference voltage output.
15	PGOOD	Power good signal open−drain output.
16	OCDDQ	Overcurrent sense and program input for the high−side FET of VDDQ regulator. Also the battery voltage input for the internal ramp generator to implement the voltage feedforward rejection to the input voltage variation.
17	BOOST	Positive supply input for high−side gate driver of VDDQ regulator and boost capacitor connection.
18	TGDDQ	Gate driver output for VDDQ regulator high−side N−Channel power FET.
19	SWDDQ	VDDQ regulator inductor driven node, return for high−side gate driver, and current limit sense input.
20	VCCP	Power supply for the VDDQ regulator low−side gate driver and also supply voltage for the bootstrap capacitor of the VDDQ regulator high−side gate driver supply.
21	BGDDQ	Gate driver output for VDDQ regulator low−side N−Channel power FET.
22	PGND	Power ground for the VDDQ regulator.
23	THPAD	Copper pad on bottom of IC used for heatsinking. This pin should be connected to the ground plane under the IC.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11, 20) to AGND (Pin 9)	V_{CCA}, V_{CCP}	−0.3, 6.0	V
High−Side Gate Drive Supply: BOOST (Pin 17) to SWDDQ (Pin 19) High−Side FET Gate Drive Voltage: TGDDQ (Pin 18) to SWDDQ (Pin 19)	V_{BOOST}−V_{SWDDQ}, V_{TGDDQ}−V_{SWDDQ}	−0.3, 6.0	V
Input/Output Pins to AGND (Pin 9) Pins 1−4, 6−8, 10, 12−15, 21	V_{IO}	−0.3, 6.0	V
Overcurrent Sense Input (Pin 16) to AGND (Pin 9)	V_{OCDDQ}	27	V
Switch Node (Pin 19)	V_{SWDDQ}	−4.0 (<100 ns), 0.3 (dc), 32	V
PGND (Pin 22), VTTGND (Pin 5) to AGND (Pin 9)	V_{GND}	−0.3, 0.3	V
Thermal Characteristics DFN−22 Plastic Package Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	2	−

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤2.0 kV per JEDEC standard: JESD22–A114.
   Machine Model (MM) ≤200 V per JEDEC standard: JESD22–A115.
2. Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, T_A = −40 to 85°C, V_{CCA} = V_{CCP} = V_{BOOST} − V_{SWDDQ} = 5.0 V, L = 1.8 μH, C_{OUT1} = 150 μF x 2, C_{OUT2} = 22 μF x 2, RL1 = 1.0 kΩ, R1 = 4.3 kΩ, R2 = 3.3 kΩ, RZ1 = 6.2 kΩ, RZ2 = 130 Ω, CP1 = 100 pF, CZ1 = 2.2 nF, CZ2 = 4.7 nF, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
Input Voltage	V_{IN}	−	4.5	−	24	V
V_{CCA} Operating Voltage	V_{CCA}	−	4.5	5.0	5.5	V
V_{CCP} Operating Voltage	V_{CCP}	−	4.5	5.0	5.5	V
SUPPLY CURRENT						
V_{CCA} Quiescent Supply Current in S0	I_{VCCA_S0}	V_{DDQEN} = 5.0 V, V_{TTEN} = 5.0 V	−	5.0	10	mA
V_{CCA} Quiescent Supply Current in S3	I_{VCCA_S3}	V_{DDQEN} = 5.0 V, V_{TTEN} = 0 V	−	−	5.0	mA
V_{CCA} Shutdown Current	I_{VCCA_SD}	V_{DDQEN} = 0 V, V_{TTEN} = 0 V	−	−	4.0	μA
V_{CCP} Quiescent Supply Current in S0	I_{VCCP_S0}	V_{DDQEN} = 5.0 V, V_{TTEN} = 5.0 V, TGDDQ and BGDDQ Open	−	−	20	mA
V_{CCP} Quiescent Supply Current in S3	I_{VCCP_S3}	V_{DDQEN} = 5.0 V, V_{TTEN} = 0 V, TGDDQ and BGDDQ Open	−	−	20	mA
V_{CCP} Shutdown Current	I_{VCCP_SD}	V_{DDQEN} = 0 V, V_{TTEN} = 0 V	−	−	1.0	μA
UNDERVOLTAGE MONITOR						
V_{CCA} UVLO Lower Threshold	V_{CCAUV-}	Falling Edge	−	3.7	4.1	V
V_{CCA} UVLO Hysteresis	$V_{CCAUVHYS}$	−	−	0.35	−	V
V_{OCDDQ} UVLO Upper Threshold	$V_{OCDDQUV+}$	Rising Edge	−	3.5	−	V
V_{OCDDQ} UVLO Hysteresis	$V_{OCDDQUVHYS}$	−	−	0.2	−	V
THERMAL SHUTDOWN						
Thermal Trip Point	T_{SD}	(Note 3)	−	150	−	°C
Hysteresis	T_{SDHYS}	(Note 3)	−	25	−	°C
V_{DDQ} SWITCHING REGULATOR						
FBDDQ Feedback Voltage, Control Loop in Regulation	V_{FBDDQ}	T_A = 25°C T_A = −40 to 85°C	0.788 0.780	0.8 0.8	0.812 0.820	V
Feedback Input Current	I_{fb}	V_{FBDDQ} = 0.8 V	−	−	1.0	μA
Oscillator Frequency	F_{SW}	−	340	400	460	kHz
Ramp Amplitude Voltage	V_{ramp}	V_{IN} = 5.0 V (Note 3)	−	1.25	−	V
Ramp Amplitude to V_{IN} Ratio	dVRAMP/dVIN	−	−	45	−	mV/V
OCDDQ Pin Current Sink	I_{OC}	V_{OCDDQ} = 4.0 V	23	35	47	μA
OCDDQ Pin Current Sink Temperature Coefficient	TC_{IOC}	T_A = −40 to 85°C	−	3200	−	ppm/°C
Minimum On Time	t_{onmin}	−	−	150	−	ns
Maximum Duty Cycle	D_{max}	V_{IN} = 5.0 V V_{IN} = 15 V V_{IN} = 24 V	− − −	90 50 32	− − −	%
Soft−Start Current	I_{ss}	V_{DDQEN} = 5.0 V, Vss = 0 V	3.5	5.0	6.5	μA
Overvoltage Trip Threshold	FBOVPth	With Respect to Error Comparator Threshold of 0.8 V	115	130	−	%
Undervoltage Trip Threshold	FBUVPth	With Respect to Error Comparator Threshold of 0.8 V	−	65	75	%

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) (V_{IN} = 12 V, T_A = −40 to 85°C, V_{CCA} = V_{CCP} = V_{BOOST} − V_{SWDDQ} = 5.0 V, L = 1.8 μH, C_{OUT1} = 150 μF x 2, C_{OUT2} = 22 μF x 2, RL1 = 1.0 kΩ, R1 = 4.3 kΩ, R2 = 3.3 kΩ, RZ1 = 6.2 kΩ, RZ2 = 130 Ω, CP1 = 100 pF, CZ1 = 2.2 nF, CZ2 = 4.7 nF, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
DC Gain	GAIN	(Note 4)	−	70	−	dB
Unity Gain Bandwidth	Ft	COMP_GND = 220 nF, 1.0 Ω in Series (Note 4)	−	2.0	−	MHz
Slew Rate	SR	(Note 4)	−	3.0	−	V/μS
GATE DRIVERS						
TGDDQ Gate Pull−HIGH Resistance	R_{H_TG}	V_{BOOST} − V_{SWDDQ} = 5.0 V, V_{TGDDQ} − V_{SWDDQ} = 4.0 V	−	1.8	−	Ω
TGDDQ Gate Pull−LOW Resistance	R_{L_TG}	V_{BOOST} − V_{SWDDQ} = 5.0 V, V_{TGDDQ} − V_{SWDDQ} = 1.0 V	−	1.8	−	Ω
BGDDQ Gate Pull−HIGH Resistance	R_{H_BG}	V_{CCP} = 5.0 V, V_{BGDDQ} = 4.0 V	−	1.8	−	Ω
BGDDQ Gate Pull−LOW Resistance	R_{L_BG}	V_{CCP} = 5.0 V, V_{BGDDQ} = 1.0 V	−	0.9	−	Ω
V_{TT} ACTIVE TERMINATOR						
V_{TT} with Respect to 1/2V_{DDQREF}	d_{VTT0}	1/2VDDQREF – V_{TT}, VDDQREF = 2.5 V, I_{VTT} = 0 to 2.4 A (Sink Current)	−30	−	−	mV
		I_{VTT} = 0 to –2.4 A (Source Current)	−	−	30	
		1/2VDDQREF – V_{TT}, VDDQREF = 1.8 V, I_{VTT} = 0 to 2.0 A (Sink Current)	−30	−	−	mV
		I_{VTT} = 0 to –2.0 A (Source Current)	−	−	30	
DDQREF Input Resistance	DDQREF_R	−	−	50	−	kΩ
Source Current Limit	$I_{LIMVTsrc}$	−	2.5	3.0	−	A
Sink Current Limit	$I_{LIMVTsnk}$	−	2.5	3.0	−	A
Soft−Start Source Current Limit	$I_{LIMVTSS}$	−	−	1.0	−	A
Maximum Soft−Start Time	$t_{ssvttmax}$	−	−	1.0	−	ms
V_{TTREF} OUTPUT						
V_{TTREF} Source Current	I_{VTTR}	VDDQREF = 1.8 V or 2.5 V	15	−	−	mA
V_{TTREF} Accuracy Referred to 1/2V_{DDQREF}	d_{VTTR}	1/2VDDQREF – V_{TTR}, VDDQREF = 2.5 V, I_{VTTR} = 0 mA to 15 mA	−25	−	25	mV
		1/2VDDQREF – V_{TTR}, VDDQREF = 1.8 V, I_{VTTR} = 0 mA to 15 mA	−18	−	18	mV

4. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) (V_{IN} = 12 V, T_A = −40 to 85°C, V_{CCA} = V_{CCP} = V_{BOOST} − V_{SWDDQ} = 5.0 V, L = 1.8 μH, C_{OUT1} = 150 μF x 2, C_{OUT2} = 22 μF x 2, RL1 = 1.0 kΩ, R1 = 4.3 kΩ, R2 = 3.3 kΩ, RZ1 = 6.2 kΩ, RZ2 = 130 Ω, CP1 = 100 pF, CZ1 = 2.2 nF, CZ2 = 4.7 nF, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
CONTROL SECTION						
VDDQEN Pin Threshold High	V_{DDQEN_H}	−	1.4	−	−	V
VDDQEN Pin Threshold Low	V_{DDQEN_L}	−	−	−	0.5	V
VDDQEN Pin Input Current	I_{IN_VDDQEN}	V_{DDQEN} = 5.0 V	−	−	0.5	μA
VTTEN Pin Threshold High	V_{TTEN_H}	−	1.4	−	−	V
VTTEN Pin Threshold Low	V_{TTEN_L}	−	−	−	0.5	V
VTTEN Pin Input Current	I_{IN_VTTEN}	V_{DDQEN} = V_{TTEN} = 5.0 V	−	−	0.5	μA
PGOOD Pin ON Resistance	PGOOD_R	$I_{\_PGOOD}$ = 5.0 mA	−	80	−	Ω
PGOOD Pin OFF Current	PGOOD_LK	−	−	−	1.0	μA
PGOOD LOW−to−HIGH Hold Time, for S5 to S0	t_{hold}	(Note 5)	−	−	200	μs

5. Guaranteed by design, not tested in production.

DETAILED OPERATING DESCRIPTION

General

The NCP5214 2−in−1 Notebook DDR Power Controller combines the efficiency of a PWM controller for the VDDQ supply, with the simplicity of using a linear regulator for the VTT termination voltage power supply. The VDDQ output can be adjusted through the external potential divider, while the VTT is internally set to track half VDDQ.

The inclusion of VDDQ power good voltage monitor, soft−start, VDDQ overcurrent protection, VDDQ overvoltage and undervoltage protections, supply undervoltage monitor, and thermal shutdown makes this device a total power solution for high current DDR memory system. The IC is packaged in DFN−22.

Control Logic

The internal control logic is powered by VCCA. The IC is enabled whenever VDDQEN is high (exceed 1.4 V). An internal bandgap voltage, VREF, is then generated. Once VREF reaches its regulation voltage, an internal signal VREFGD will be asserted. This transition wakes up the supply undervoltage monitor blocks, which will assert VCCAGD if VCCA voltage is within certain preset levels.

The control logic accepts external signals at VCCA, OCDDQ, VDDQEN, VTTEN, and $\overline{\text{FPWM}}$ pins to control the operating state of the VDDQ and VTT regulators in accordance with Table 1. A timing diagram is shown in Figure 3.

VDDQ Switching Regulator in Normal Mode (S0)

The VDDQ regulator is a switching synchronous rectification buck controller directly driving two external N−Channel power FETs. An external resistor divider sets the nominal output voltage. The control architecture is voltage mode fixed frequency PWM with external compensation and with switching frequency fixed at 400 kHz ± 15%. As can be observed from Figure 1, the VDDQ output voltage is divided down and fed back to the inverting input of an internal error amplifier through FBDDQ pin to close the loop at VDDQ = VFBDDQ × (1 + R2/R1). This amplifier compares the feedback voltage with an internal VREF (= 0.800 V) to generate an error signal for the PWM comparator. This error signal is further compared with a fixed frequency RAMP waveform derived from the internal oscillator to generate a pulse−width−modulated signal. This PWM signal drives the external N−Channel Power FETs via the TGDDQ and BGDDQ pins. External inductor L and capacitor COUT1 filter the output waveform. The VDDQ output voltage ramps up at a pre−defined soft−start rate when the IC enters state S0 from S5. When in normal mode, and regulation of VDDQ is detected, signal INREGDDQ will go HIGH to notify the control logic block.

Input voltage feedforward is implemented to the RAMP signal generation to reject the effect of wide input voltage variation. With input voltage feedforward, the amplitude of the RAMP is proportional to the input voltage.

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a diode or Schottky diode rectifier. Adaptive non−overlap timing control of the complementary gate drive output signals is provided to reduce large shoot−through current that degrades efficiency.

Tolerance of VDDQ

The tolerance of VFBDDQ and the ratio of external resistor divider R1/R2 both impact the precision of VDDQ. With the control loop in regulation, VDDQ = VFBDDQ × (1 + R1/R2). With a worst case (for all valid operating conditions) VFBDDQ tolerance of ±1.5%, a worst case range of ±2.5% for VDDQ = 1.8 V will be assured if the ratio R1/R2 is specified as 1.2500 ±1%.

Table 1. State, Operation, Input and Output Condition Table

	Input Conditions					Operating Conditions			Output Conditions		
Mode	VCCA	VOCDDQ	VDDQEN	VTTEN	$\overline{\text{FPWM}}$	VDDQ	VTTREF	VTT	TGDDQ	BGDDQ	PGOOD
S5	Low	X	X	X	X	H−Z	H−Z	H−Z	Low	Low	Low
S5	X	Low	X	X	X	H−Z	H−Z	H−Z	Low	Low	Low
S0	High	High	High	High	X	Normal	Normal	Normal	Normal	Normal	H−Z
S3	High	High	High	Low	High	Standby	Normal	H−Z	Standby (Power−saving)	Standby (Power−saving)	H−Z
S3	High	High	High	Low	Low	Normal	Normal	H−Z	Normal	Normal	H−Z
S5	X	X	Low	X	X	H−Z	H−Z	H−Z	Low	Low	Low

VDDQ Regulator in Standby Mode (S3)

During state S3, a power−saving mode is activated when the $\overline{\text{FPWM}}$ pin is pulled to VCCA. In power−saving mode, the switching frequency is reduced with the VDDQ output current and the low−side FET is turned off after the detection of negative inductor current, so as to enhance the efficiency of the VDDQ regulator at light loads. The switching frequency can be reduced smoothly until it reaches the minimum frequency at about 15 kHz. Therefore, perceptible audible noise can be avoided at light load condition.

In power−saving mode, the low−side MOSFET is turned off after the detection of negative inductor current and the converter cannot sink current. The power−saving mode can be disabled by pulling the $\overline{\text{FPWM}}$ pin to ground. Then, the converter operates in forced−PWM mode with fixed switching frequency and ability to sink current.

Fault Protection of VDDQ Regulator

During state S0 and S3, external resistor (RL1) sets the current limit for the high−side switch. An internal 35 μA current sink (IOC) at OCDDQ pin establishes a voltage drop across this resistor. Besides, an offset voltage at the magnitude of RL1xIOC is also developed at the non−inverting input of the current limit comparator. The voltage at the non−inverting input is compared to the voltage at SWDDQ pin when the high−side gate drive is high after a fixed period of blanking time (150 ns) to avoid false current limit triggering. When the voltage at SWDDQ is lower than that at the non−inverting input for a consecutive 15 internal clock cycles, an overcurrent condition occurs, during which, all outputs will be latched off to protect against a short−to−ground condition on SWDDQ or VDDQ. The IC will be reset once VCCA or VDDQEN is cycled.

Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figure 2.

VTT Active Terminator in Normal Mode (S0)

The VTT active terminator is a two−quadrant linear regulator with two internal N−channel power FETs. It is capable of sinking and sourcing at least 1.5 A continuous current and up to 2.4 A transient peak current. It is activated in normal mode in state S0 when the VTTEN pin is HIGH and VDDQ is in regulation. Its input power path is from VDDQ with the internal FETs gate drive power derived from VCCA. The VTT internal reference voltage is derived from the DDQREF pin. The VTT output is set to VDDQ/2 when VTT output is connecting to the FBVTT pin directly. This regulator is stable with any value of output capacitor greater than 30 μF. The VTT regulator will have an internal soft−start when it is transited from disable to enable. During the VTT soft−start, a current limit is used as a current source to charge up the VTT output capacitor. The current limit is initially 1.0 A during VTT soft−start. It is then increased to 2.5 A after 1.0 ms or VTT output is in regulation, whichever is earlier.

VTT Active Terminator in Standby Mode (S3)

VTT output is high−impedance in S3 mode.

Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, bidirectional current limit is implemented, preset at the minimum of 2.5 A magnitude.

Thermal Consideration of VTT Active Terminator

The VTT terminator is designed to handle large transient output currents. If large currents are required for very long duration, then care should be taken to ensure the maximum junction temperature is not exceeded. The 5x6 DFN−22 has a thermal resistance of 35°C/W (dependent on air flow, grade of copper, and number of vias). *In order to take full advantage from this thermal capability of this package, the thermal pad underneath must be soldered directly onto a PCB metal substrate to allow good thermal contact.*

VTTREF Output

The VTTREF output tracks VDDQREF/2 at ±2% accuracy. It has source current capability of up to 15 mA. VTTREF should be bypassed to analog ground of the device by 1.0 μF ceramic capacitor for stable operation. The VTTREF is turned on as long as VDDQEN is pulled high. In S0 mode, VTTREF soft−starts with VDDQ and tracks VDDQREF/2. In S3 mode, VTTREF is kept on with VDDQ. VTTREF is turned off only in S4/S5 like VDDQ output.

Supply Voltage Undervoltage Monitor

The IC continuously monitors VCCA and VIN through VCCA pin and OCDDQ pin respectively. VCCAGD is set HIGH if VCCA is higher than its preset threshold (derived from VREF with hysteresis). The IC will enter S5 state if VCCA fails while in S0 and both VDDQEN and VTTEN remain HIGH.

Thermal Shutdown

When the chip junction temperature exceeds 150°C, the entire IC is shutdown. The IC resumes normal operation only after the junction temperature dropping below 125°C.

APPLICATION INFORMATION

Overcurrent Protection

The OCP circuit is configured to set the current limit for the current flowing through the high−side FET and inductor during S0 and S3. The overcurrent tripping level is programmed by an external resistor RL1 connected between the OCDDQ pin and drain of the high−side FET. An internal 35 μA current sink (IOC) at pin OCDDQ establishes a voltage drop across the resistor RL1 at a magnitude of RL1xIOC. Besides, an additional offset voltage V_{OFFSET} of 25 mV is developed at the non−inverting input of the current limit comparator. The voltage at the non−inverting input is then compared to the voltage at SWDDQ pin when the high−side gate drive is high after a fixed period of blanking time (150 ns) to avoid false current limit triggering. When the voltage at SWDDQ is lower than the voltage at the non−inverting input of the current limit comparator for a consecutive 15 internal clock cycles, an overcurrent condition occurs, during which, all outputs will be latched off to protect against a short−to−ground condition on SWDDQ or VDDQ. i.e., the voltage drop across the $R_{ds(on)}$ of high−side FET developed by the drain current is larger than the voltage drop across RL1 plus the additional offset voltage, the OCP is triggered and the device will be latched off.

The overcurrent protection will trip when a peak inductor current hit the I_{LIMIT} determined by the equation:

$$I_{LIMIT} = \frac{RL1 \times IOC + V_{OFFSET}}{R_{ds(on)}}$$

Since the MOSFET $R_{ds(on)}$ varies with temperature as current flows through the MOSFET increases, the OCP trip point will also varies with the MOSFET $R_{ds(on)}$ temperature variation. The IOC temperature coefficient of 3200 ppm is used to compensate the $R_{ds(on)}$ temperature variation.

To avoid false triggering the overcurrent protection in normal operating load range, calculate the RL1 value from the above equation with the following condition:

1. The minimum IOC value from the specification table,
2. The maximum $R_{ds(on)}$ of the MOSFET used at the highest junction temperature,
3. Determine I_{LIMIT} for $I_{LIMIT} > I_{OUT(MAX)} + \Delta I_L/2$.

Besides, a decoupling capacitor C_{DCPL} should be added closed to the lead of the current limit setting resistor RL1 which connected to the drain of the high−side MOSFET.

Soft−Start

A VDDQ soft−start feature is incorporated in the device to prevent surge current from power supply and output voltage overshot during power up. When VDDQEN, VCCA, and VOCDDQ rise above their respective upper threshold voltages, the external soft−start capacitor Css will be charged up by a constant current source, I_{ss}. When the soft−start voltage (Vcss) rises above the SS_EN voltage (~50 mV), the BGDDQ and TGDDQ will start switching and VDDQ output will ramp up. When the soft−start voltage reaches the SS_OK voltage (~Vref + 50 mV), the soft− start of VDDQ is finished. The C_{ss} will continue to charge up until it reaches about 2.5 V to 3.0 V.

The soft−start time t_{ss} can be programmed according to the following equation:

$$t_{ss} \approx \frac{0.8 \times C_{ss}}{I_{ss}}$$

Ceramic capacitors with low tolerance and low temperature coefficient, such as B, X5R, X7R ceramic capacitors are recommended to be used as the Css. Ceramic capacitors with Y5V temperature characteristic are not recommended.

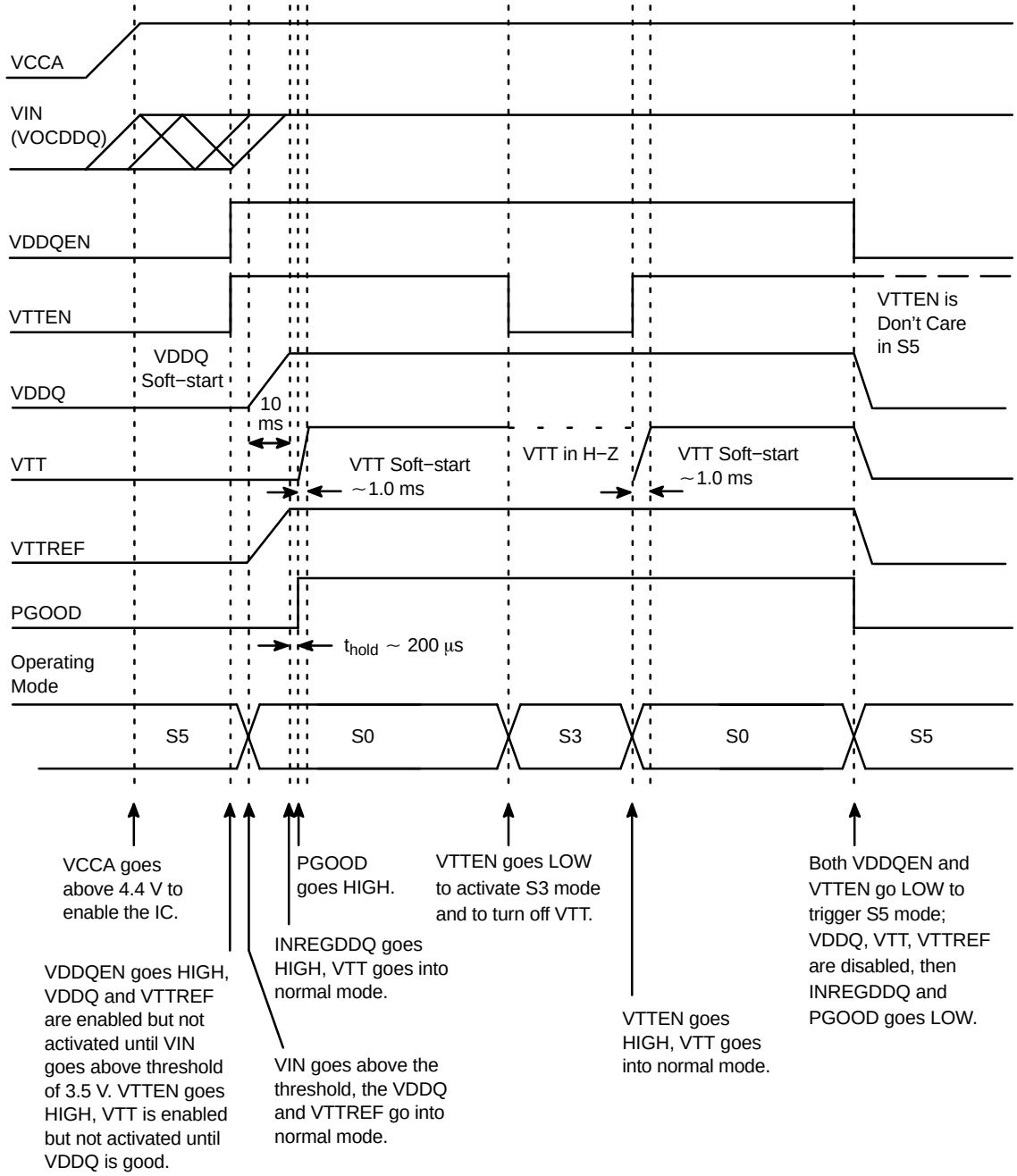
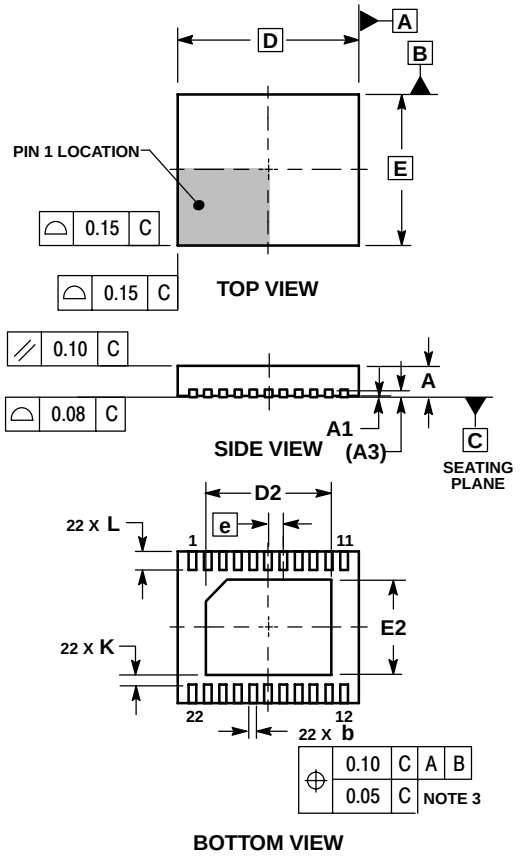


Figure 3. Powerup and Powerdown Timing Diagram

PACKAGE DIMENSIONS

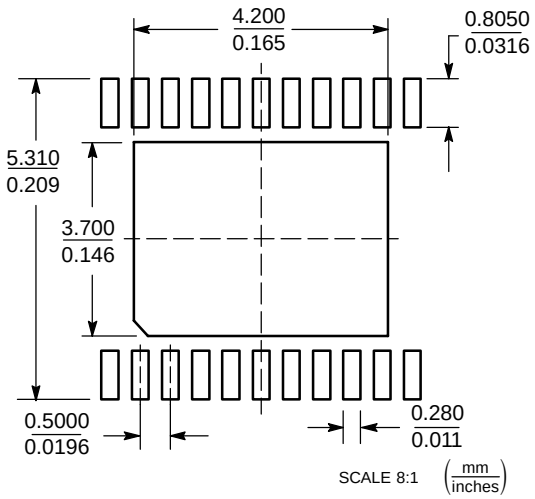
DFN−22
MN SUFFIX
CASE 506AF−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.50	0.60

SOLDERING FOOTPRINT



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