MVPG30x/MVPG31

Field Programmable DSP Switcher™

1 MHz, 3.0A Peak Current-Limit Step-Down Regulator with AnyVoltage™ Technology

Datasheet

Doc. No. MV-S102808-00, Rev. G
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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: 2.00	Technical Publication: 0.xx

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PRODUCT OVERVIEW

The Marvell® MVPG30x/MVPG31 is an intelligent digital synchronous step-down (Buck) switching regulator housed in a 4 mm x 3 mm DFN-12 package. The MVPG15x has an additional on-chip Low-Drop-Out (LDO) regulator controller. Internally self-compensated, the step-down regulator requires no external compensation and work with low-ESR output capacitors to simplify the design, minimize the board space, and reduce the amount of external components. The switching frequency for the step-down regulator is 1 MHz, allowing the use of low profile surface mount inductors and low value capacitors. The step-down regulator includes programmable output voltage to provide the user the ability to easily set the output voltage with external resistors, logic control, or serial data interface. The output voltage range is 0.72V to 3.63V.

The LDO regulator controller with an external P-Channel MOSFET forms a low dropout regulator capable of driving 800 mA output current. The output voltage of the LDO regulator is fixed.

The MVPG30x/MVPG31 operate from an input voltage range of 3.0V to 5.5V, making the device well-suited for portable applications.

Other key features of the MVPG30x/MVPG31 include an internal current limit for the step-down regulator, an Under Voltage Lockout (UVLO), and thermal shutdown.

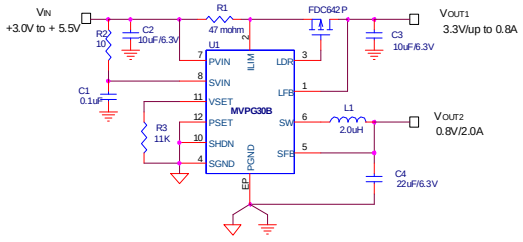
Features

- Tiny 4 mm x 3 mm DFN-12 package
- 1 MHz switching frequency
- Small and low profile inductors
- Stable with ceramic output capacitors
- No external compensation required
- Minimum amount of external components
- Over 95% efficiency
- High peak switch current limit: 3.0A
- Input voltage range: 3.0V to 5.5V
- Serial/Logic programmability
- AnyVoltage™ Technology provides 64 output voltage selections to provide flexibility
- Programmable output voltage range: 0.72V to 3.63V
- P-Channel LDO regulator controller with programmable current limit (MVPG30x)
- Lead-free packages
- Built-in under voltage lockout
- Over voltage protection
- Thermal shutdown protection
- Output voltage margining capability

Application

- Portable computing
- Point of load power supplies
- DSP power supplies
- Disk drive power supplies

Figure 1: Typical High Efficiency 5.0V to 0.8V/2.0A Step-Down Regulator with 3.3V LDO Regulator



Caution This is a very high frequency device and proper PCB layout is required. Refer to Section 6, Applications Information, on page 49 for further information.

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Figure 2: 12-Pin DFN Pin Diagram—MVPG30x Top View

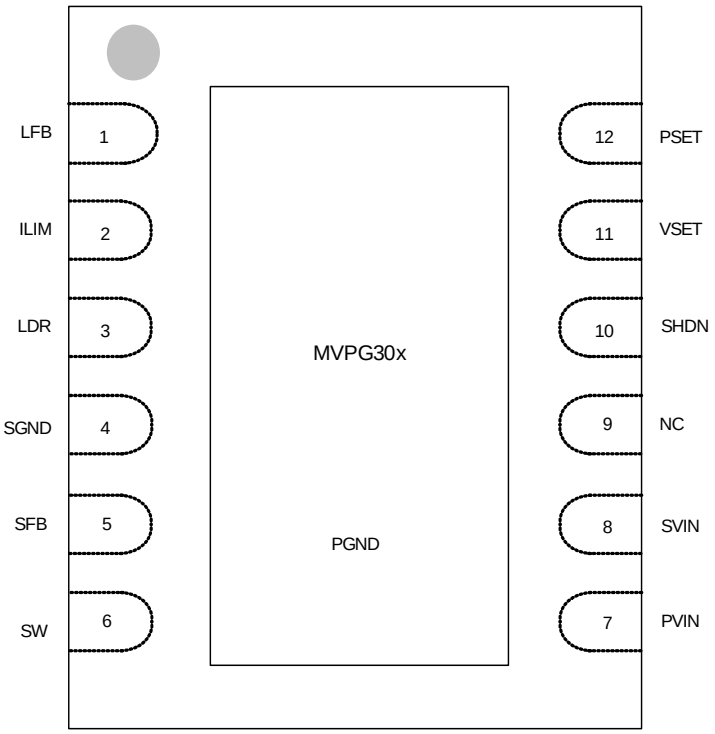
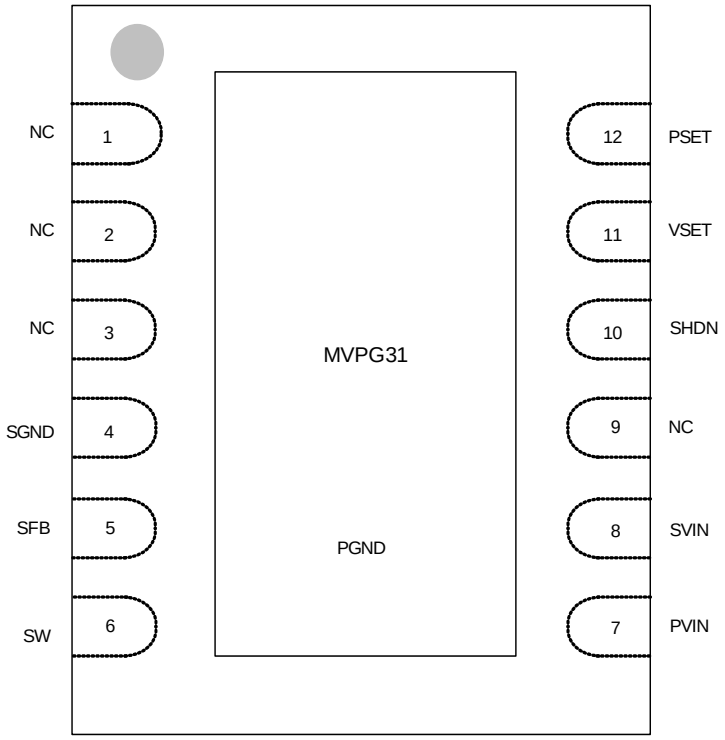


Figure 3: 12-Pin DFN Pin Diagram—MVPG31 Top View



1.2 Pin Type Definitions

Table 1: Pin Type Definitions

Pin Type	Definitions
I	Input only
O	Output only
S	Supply
NC	Not Connected
GND	Ground

1.3 Pin Description

Table 2 provides pin descriptions for the MVPG30x/MVPG31.

Table 2: Pin Description

MVPG30x Pin #	MVPG31 Pin #	Pin Name	Pin Type	Pin Function
1	--	LFB	I	LDO Regulator Controller Feedback Senses the output voltage of the LDO regulator. Connect to the drain of the P-channel MOSFET. When the LDO controller is not used, float the LDR pin. Connect the LFB to SGND, and connect ILIM to SVIN.
2	--	ILIM	I	Current-Limit Sense Pin for the LDO Regulator A built-in offset of 50 mV (typical) between V_{IN} and ILIM in conjunction with the sense resistor is used to set the current-limit threshold for the LDO regulator controller. Connecting this pin to V_{IN} disables the internal current limit circuitry. When the LDO controller is not used, float the LDR pin. Connect the LFB to SGND, and connect ILIM to SVIN.
3	--	LDR	O	LDO Regulator Controller Driver Connect to the gate of an external P-channel MOSFET. The external P-Channel MOSFET needs to have a threshold of -2.5V or lower and input capacitance (C_{iss}) of less than 1000 pF. When the LDO controller is not used, float the LDR pin. Connect the LFB to SGND, and connect ILIM to SVIN.
4	4	SGND	O	Signal Ground This pin must connect to the power ground.
5	5	SFB	I	Switching Regulator Feedback Senses the output voltage of the switching regulator.
6	6	SW	O	Switch Node Internal power MOSFET drain. This pin must connect to an external inductor.

Table 2: Pin Description (Continued)

MVPG30x Pin #	MVPG31 Pin #	Pin Name	Pin Type	Pin Function
7	7	PVIN	I	Power Input Voltage Internal power MOSFET source. Connect the decoupling 10 µF capacitors between PVIN and PGND and position it as close as possible to the IC.
8	8	SVIN	I	Signal Input Voltage Input voltage is 3.0V to 5.5V for internal circuitry. Connect a 0.1 µF decoupling capacitor between SVIN and SGND and position it as close as possible to the IC.
9	1, 2, 3, 9	NC	O	No Connect This pin is left floating. Do not connect this pin.
10	10	SHDN	I	Shutdown Logic low (≤0.8V) enables the step-down switching regulator and the LDO regulator controller. Logic high (≥2.0V) disables the step-down switching regulator and the LDO regulator controller. The high signal duration has to be at least 20 µs to disable both regulators.
11	12	VSET	I	Voltage Set 1. Connect an external resistor to ground to set the output voltage of the step-down switching regulator. See Table 5, Electrical Characteristics, on page 19 for resistor values and output voltage options. 2. The total capacitance across this pin and SGND should not be greater than 25 pF. Shorting this pin to signal ground, floating this pin, or using 619 kΩ< R_{VSET} or R_{VSET}<7.68 kΩ disables the step-down switching regulator and sets the SFB pin to high impedance. Use resistor value with tolerance better than 2%.
12	12	PSET	I	Percent Set 1. Connect an external resistor to ground to set the output voltage of the step-down switching regulator. See Table 5, Electrical Characteristics, on page 19 for resistor values and output voltage options. 2. The total capacitance across this pin and SGND should not be greater than 25 pF. Shorting this pin to signal ground, floating this pin, or using 619 kΩ< R_{PSET} or R_{PSET}<7.68 kΩ does not affect the set voltage. Use resistor value with tolerance better than 2%. Although this pin can be left floating when it is not used, it is recommended to connect this pin to ground.
Exposed Pad	Exposed Pad	PGND	GND	Power Ground The power ground must connect to the negative terminal of the input and output capacitors.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings[1]

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units
PV_{IN} to PGND	-0.3	--	6.0	V
PV_{IN} to SV_{IN}	-0.3	--	+0.3	V
PGND to SGND	-0.3	--	+0.3	V
V_{SW} to PGND[2]	-0.3	--	(PV_{IN} +0.3)	V
V_{SFB} to SGND	-0.3	--	(SV_{IN} +0.3)	V
V_{VSET}, V_{PSET} to SGND	-0.3	--	(SV_{IN} +0.3)	V
V_{ILIM}, V_{LDR}, V_{LFB} to SGND	-0.3	--	(SV_{IN} +0.3)	V
V_{SHDN} to SGND	-0.3	--	(SV_{IN} +0.3)	V
Operating Ambient Temperature Range[3]	-40	--	85	°C
Maximum Junction Temperature	--	--	150	°C
Storage Temperature Range	-65	--	150	°C
Lead Temperature (soldering, 10s)	--	300	--	°C
ESD Rating[4]	--	2.0	--	kV

1. Exceeding the absolute maximum rating may damage the device.
2. Capable of -1.0V for less than 50 ns.
3. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ, in series with 100 pF.

2.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Units
SV_{IN}	Signal Input Voltage	3.0	--	5.5	V
PV_{IN}	Power Input Voltage	3.0	--	5.5	V
θ_{JA}	Package Thermal Resistance[2]	--	48.1	--	°C/W
θ_{JC}		--	4.4	--	°C/W
T_{JMAX}	Maximum Operating Junction Temperature	--	--	125	°C

1. This device is not guaranteed to function outside the specified operating range.
2. Tested on 4-layer (JESD51-7) and vias (JESD51-5) boards.

2.3 Electrical Characteristics

Table 5: Electrical Characteristics

NOTE: The following applies unless otherwise noted: SV_{IN} = PV_{IN} = 5.0V, V_{SHDN} = SGND = PGND, $L_{(BUCK)}$ = 2.0 µH, $C_{OUT(BUCK)}$ = 22 µF (Ceramic), PFET = FDC642P, $C_{OUT(LDO)}$ = 10 µF (Ceramic), T_A = 25°C. **Bold values indicate -40°C ≤ T_A ≤ 85°C**.

Symbol	Parameter	Conditions	Min	Type	Max	Units
SV_{IN}	Input Voltage Range	SV_{IN} = PV_{IN}	**3.0**	**--**	**5.5**	V
	Total Quiescent Current	No load, V_{OUT} = TBD	--	1.3	--	mA
I_{SVIN}	Shutdown Supply Current	V_{SHDN} = SV_{IN} = 5.5V	--	1.0	10	µA
V_{UVLO}	Under Voltage Lockout	High threshold, SV_{IN} increasing, I_{LOAD} = 10mA	--	2.65	**2.85**	V
		Low threshold, SV_{IN} decreasing, I_{LOAD} = 10mA	**2.35**	2.50	**--**	V
V_{OVP}	Over Voltage Protection	High threshold, SV_{IN} increasing, I_{LOAD} = 10mA	--	5.7	TBD	V
		Low threshold, SV_{IN} decreasing, I_{LOAD} = 10mA	TBD	5.6	--	V
V_{SHDN}	Shutdown Input Voltage Logic	Enable regulators	--	--	**0.8**	V
		Disable regulators	**2.0**	--	--	
I_{SHDN}	Shutdown Input Current	V_{SHDN} = SGND = PGND or 5.5V	--	--	±1.0	µA
T_{OTS}	Over-temperature Thermal Shutdown	T_J increasing (Disable regulators)	--	150	--	°C
		T_J decreasing (Enable regulators)	--	120	--	°C

2.4 Switching Step-down Regulator

Table 6: Switching Step-down Regulator

NOTE: The following applies unless otherwise noted: SV_{IN} = PV_{IN} = 5.0V, V_{PSET} = V_{SHDN} = SGND = PGND, R_{VSET} = 11 kΩ, L = 2.0 µH, C_{OUT} = 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40°C ≤ T_A ≤ 85°C**.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Output Voltage	R_{VSET} = 11K, PWM mode	--	0.8	--	V
		R_{VSET} = 18.7K, PWM mode	--	1.0	--	
		R_{VSET} = 31.6K, PWM mode	--	1.2	--	
		R_{VSET} = 53.6K, PWM mode	--	1.5	--	
		R_{VSET} = 97.6K, PWM mode	--	1.8	--	
		R_{VSET} = 165K, PWM mode	--	2.5	--	
		R_{VSET} = 280K, PWM mode	--	3.0	--	
		R_{VSET} = 475K, PWM mode	--	3.3	--	
	Percentage Set	R_{PSET} = 11K	--	-10	--	%
		R_{PSET} = 18.7K	--	-7.5	--	
		R_{PSET} = 31.6K	--	-5.0	--	
		R_{PSET} = 53.6K	--	-2.5	--	
		R_{PSET} = 97.6K	--	2.5	--	
		R_{PSET} = 165K	--	5.0	--	
		R_{PSET} = 280K	--	7.5	--	
		R_{PSET} = 475K	--	10	--	
V_{LNREG}	Output Voltage Line Regulation	SV_{IN} = PV_{IN} = 3.0V to 5.0V V_{OUT} = 1.5V I_{LOAD} = 500 mA	--	0.1	--	%
V_{LDREG}	Output Voltage Load Regulation	SV_{IN} = PV_{IN} = 5.0V V_{OUT} = 1.5V I_{LOAD} = 500 mA to 2.0A	--	0.2	--	%
f_{SW}	Switching Frequency	PWM mode	--	1.0	--	MHz
R_{PFET}	$R_{DS(ON)}$ = of P-Channel FET	SV_{IN} = 3.0V, I_{SW} = 100 mA	--	150	--	mΩ
		SV_{IN} = 5.0V, I_{SW} = 100 mA	--	120	--	
R_{NFET}	$R_{DS(ON)}$ = of N-Channel FET	SV_{IN} = 3.0V, I_{SW} = 100 mA	--	90	--	mΩ
		SV_{IN} = 5.0V, I_{SW} = 100 mA	--	70	--	
I_{LIM}	Minimum Peak Switch Current Limit		--	TBD	--	A

Table 6: Switching Step-down Regulator (Continued)

NOTE: The following applies unless otherwise noted: SV_{IN} = PV_{IN} = 5.0V, V_{PSET} = V_{SHDN} = SGND = PGND, R_{VSET} = 11 kΩ, L = 2.0 µH, C_{OUT} = 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40°C ≤ T_A ≤ 85°C**.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LSW}	Switch Leakage Current	SV_{IN} = PV_{IN} = V_{SHDN} = 5.5V V_{SW} = PGND or 5.5V	--	±1	±50	µA

2.5 LDO Regulator Controller

Table 7: LDO Regulator Controller

NOTE: The following applies unless otherwise noted: SV_{IN} = PV_{IN} = 5.0V, V_{SHDN} = SGND = PGND, PFET= FDC642P, C_{OUT} = 10 µF, T_A = 25 °C. **Bold values indicate -40°C ≤ T_A ≤ 85°C.**

Symbol	Parameter	Conditions	Min	Type	Max	Units
	Output Voltage Accuracy	Room Temp, I_{LOAD} = 10 mA	--	±1	--	%
		Over Temp, I_{LOAD} = 10 mA	--	±2	--	
V_{LNREG}	Line Regulation	SV_{IN} = PV_{IN} = 3.5V to 5.0V, V_{OUT} = 3.3V, I_{LOAD} = 10 mA	--	0.08	--	%
V_{LDREG}	Load Regulation	SV_{IN} = PV_{IN} = 5.0V, V_{OUT} = 3.3V, I_{LOAD} = 10 mA to 800 mA	--	0.05	--	%
V_{ILTH}	Current-Limit Threshold	SV_{IN}-V_{ILIM}	--	50	--	mV

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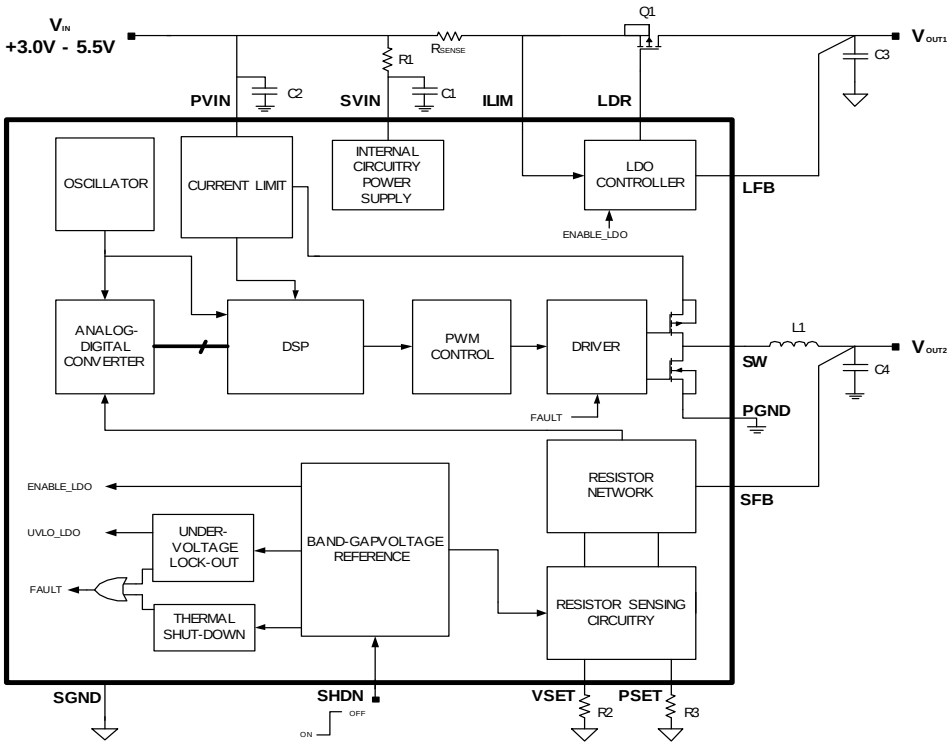
3 Functional Description

Figure 4: MVPG30x/MVPG31 Block Diagram

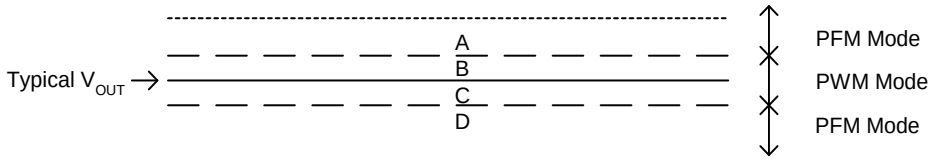


3.1 Regulation and Startup

The step-down switching regulator uses Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) modes to regulate the output voltage using digital control. The mode of operation depends on the level of output current and the output voltage.

In steady states, the step-down switching regulator monitors the current flowing through the inductor to determine if the regulator is handling heavy or light load applications. For heavy load applications, the step-down regulator operates in the PWM mode (B and C) to minimize the ripple current for optimum efficiency and to minimize the ripple output voltage. The step-down regulator operates in the PFM and Discontinuous Conduction Mode (DCM) (A and D) to limit the switching actions for optimum efficiency in light load applications. In this mode, the average output voltage is slightly higher than the average output voltage for heavy transient load applications.

Figure 5: Output Voltage Window



3.1.1 Digital Soft Start

During startup, the MVPG30x/MVPG31 provides a soft start function. Soft start reduces surge currents from the input voltage and provides well-controlled output voltage rise characteristics. The rate of the output voltage startup is limited by the value of the output capacitor and the internal current limit circuitry. This combination forces the output voltage to ramp up slowly, providing a soft start characteristic.

During soft start, the MVPG30x/MVPG31 feeds a constant current to the output capacitor in several steps. Figure 6 shows the inductor current waveform during startup. The current limit is ramped up in seven steps beginning at approximately 40% of the current limit rating and ending at 100% at 25 µs per step. The buck regulator behaves like a current source during this time as the output ramps up slowly.

Figure 7 shows that the rise time for a MVPG30x/MVPG31 increases from 20 µs at for a 0.8V output to 70 µs for a 3.3V output with a 20 mA load. From Figure 8, the rise time can be estimated by assuming an average charging current of 0.75A. Rise time with a 3.3V output is calculated using the following equation.

$$RiseTime = \frac{Cout \bullet Vout}{I}$$

$$= \frac{22\mu F \bullet 3.3V}{0.75A} = 96.8\mu s$$

Figure 6: Inductor Current Steps at Startup

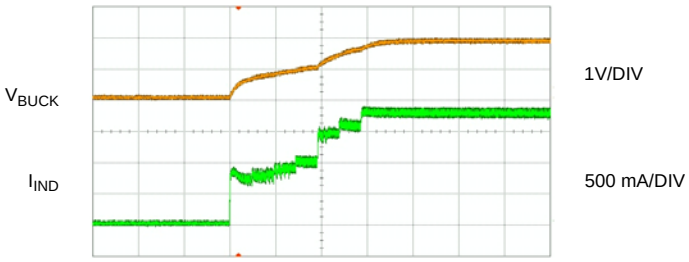


Figure 7: Soft Startup (0.8V, 1.2V, 1.8V, 2.5V, 3.3V)

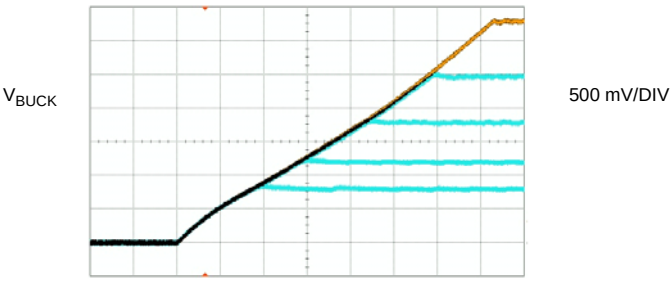
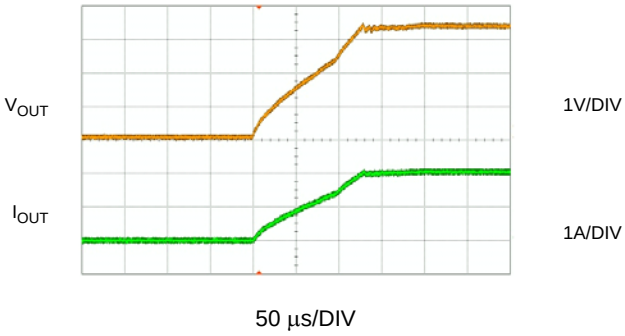


Figure 8: Soft Startup



3.2 Output Voltage—AnyVoltage™ Technology

The output voltage of the step-down switching regulator is programmed by using Table 8 to select resistor values for VSET and PSET pin. The VSET pin sets the output voltage and the PSET pin trims the set voltage to a percentage value. For example, to program 2.25V output, a 165 kΩ resistor is selected for the VSET pin, and an 11 kΩ resistor is selected for the PSET pin. The 165 kΩ resistor sets the output voltage to 2.5V and the 11 kΩ resistor trims the set voltage by -10%.

Using the VSET resistor's value greater than 619 kΩ or less than 7.68 kΩ disables the step-down switching regulator and sets the SW pin to high impedance. If the VSET resistor's value is outside the 2% tolerance, the output can be either higher or lower than the set voltage.

Using resistor values greater than 619 kΩ or less than 7.68 kΩ for the PSET pin does not affect the set voltage. When the PSET pin is not used, it must be connected to ground. Like the VSET resistor, the percent value can be either higher or lower if the PSET resistor's value is outside the 2% tolerance.

Table 8: AnyVoltage™ Programming Table for 1% Resistors

		PSET								
		-10.0%	–7.5%	–5.0%	–2.5%	0%	2.5%	5.0%	7.5%	10.0%
		11k	18.7k	31.6k	53.6k	GND	97.6k	165k	280k	475k
VSET	GND	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	11k	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
	18.7k	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
	31.6k	1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
	53.6k	1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
	97.6k	1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
	165k	2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
	280k	2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
	475k	2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630
	Open	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

The VSET and PSET resistors are read once during startup before the output voltage is turned on. The output voltage cannot be changed on-the-fly. To configure the output to a different voltage, power has to recycle or the MVPG30x/MVPG31 has to turn OFF and back ON using the shutdown pin.

Figure 9 shows the startup waveforms of the MVPG30x/MVPG31. Once the input voltage (V_{IN}) is above the Under Voltage Lockout (UVLO) Upper Threshold (UTH), the VSET and PSET pin become active. Current is first sourced out of PSET pin and then the VSET pin, in exponentially increasing steps. After each step there is a blanking time before the VSET voltage is compared to an internal 1.2V reference. If the VSET voltage is below internal reference voltage, the current source proceeds to the next step. Once the VSET voltage is above the internal reference voltage the sequence stops and the output voltage (V_{OUT}) is allowed to turn on. Figure 10 shows the VSET waveform for VSET = 2.5V and PSET = –5% output. The MVPG30x/MVPG31 keeps track of how many steps are

required to determine the appropriate output voltage. Table 9 provides the number of steps necessary for each output voltage option. Using a VSET resistor of 165 kΩ requires the current source to step four times, and a PSET resistor of 31.6 kΩ requires seven steps.

Figure 9: Startup Sequence

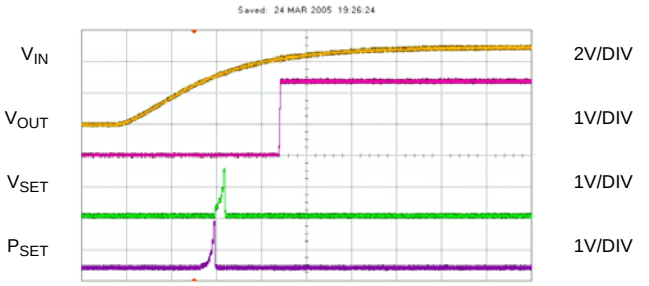


Figure 10: V_{SET} = 2.5V and P_{SET} = -5%

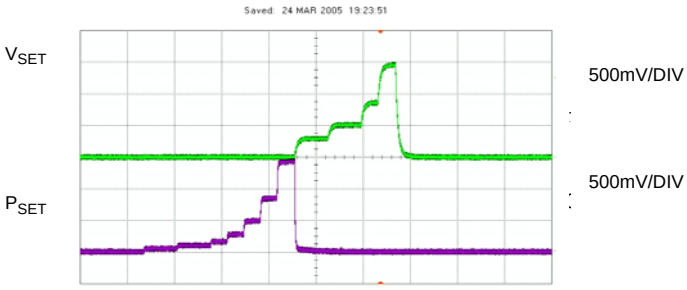


Table 9: Output Voltage Option Steps

Step	VOUT (V)	R_{VSET} (kΩ)
1	0	0
2	3.3	475
3	3.0	280
4	2.5	165
5	1.8	97.6
6	1.5	53.6
7	1.2	31.6
8	1.0	18.7
9	0.8	11

Step	PSET (%)	R_{PSET} (kΩ)
1	0	0
2	+10	475
3	+7.5	280
4	+5.0	165
5	+2.5	97.6
6	-2.5	53.6
7	-5.0	31.6
8	-7.5	18.7
9	-10	11

The MVPG30x/MVPG31 provides an innovative technique to set the output voltage. During startup it reads the value of external resistors, which are located outside the regulator's feedback loop to program the output voltage. By placing the output voltage programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. Normally, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. Whereas, the MVPG30x/MVPG31 initial accuracy is 2% for any of the eight output voltages.

The VSET and PSET pins are sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination, which introduces excessive leakage current on the VSET and PSET pin, especially for the 3.3V output or +10%. The parasitic resistance on these nodes must be greater than 3 MΩ and the stray capacitance must be less than 25 pF; otherwise, a 3.3V output can potentially end up at 3V.

3.3 Programmable Current Limit for the LDO Regulator Controller

A sense resistor is placed between SVIN and ILIM pin to program the current limit of the LDO regulator controller. The following equation is used to determine the value of the sense resistor.

$$I_{LIM} = \frac{50mV(Typical)}{R_{SENSE}(m\Omega)}$$

When the LDO regulator controller is in current limit, the internal current-limit circuitry turns off the LDO regulator controller and holds the LDO regulator controller in the off state for 3 ms (typical hold time). After the hold-time is expired, the LDO regulator controller is enabled. The current-limit circuitry continues to disable and enable the regulator until the current limit is removed.

The LDO regulator P-channel MOSFET can be selected from the following list based on the required current and ambient temperature.

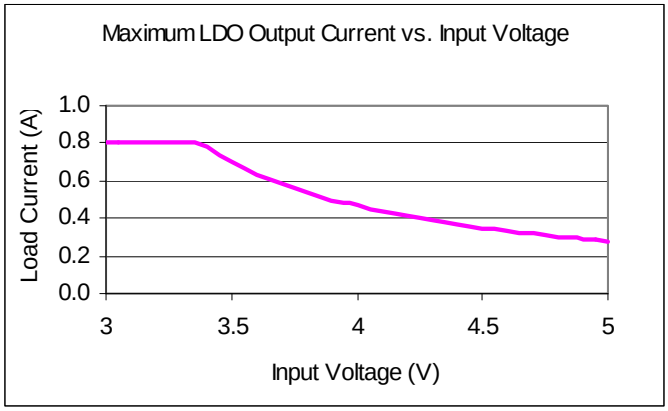
Table 10: P-Channel MOSFET Selection

Package	Vishay	Fairchild
Super SOT-6		FDC642P FDC634P
Super SOT-3 / micro 3		FDN340P FDN302P
SO-8	Si4433DY	FDS9431A
SC75-6 FLMP		FDJ127P
TO-263AB (D^2-Pack)		FDP4020P
TSOP-6	Si3443DV	
SC70-6		FDG330P
SOT-23	Si2333DS	
1206-8 Chip FET	Si5473DC	
SC-89 (6-lead)	Si1039X	
SC75A/SC-89 (3-lead)	Si1012R/X	

3.3.1 Maximum LDO Output Current

The FDS642P is design to provide up to 800 mA of continuous output current. However, the tiny Super SOT-6 package can dissipate up to 0.7W. If the input and output voltage are close, then the full 800 mA is achieved (see Figure 11). As the input voltage increases, the IC dissipates more power, limiting the maximum output current. The output current has to decrease in order to keep the power dissipation under its 0.7W limit.

Figure 11: Maximum Output Current for the FDS642P P-Channel MOSFET



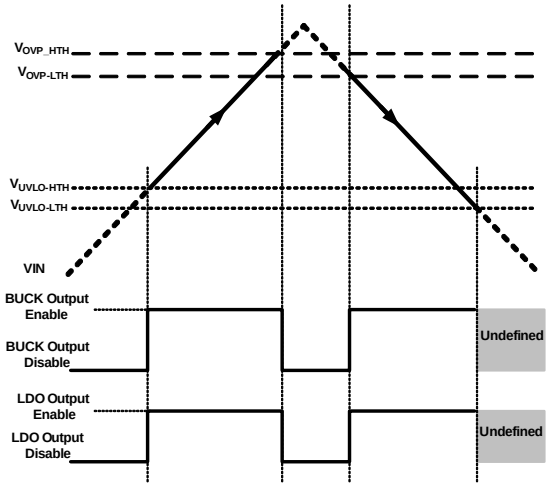
3.4 Under Voltage Lockout

At startup, the MVPG30x/MVPG31 incorporates Under Voltage Lockout (UVLO) circuitry to enable the step-down switching regulator and the LDO controller when the input voltage is above 2.60V (typical). After the MVPG30x/MVPG31 is enabled and the input voltage is lowered, the highest value of the minimum input voltage for both regulators to remain enabled is 2.50V (typical).

3.5 Over Voltage Protection

The MVPG30x/MVPG31 incorporates an Over Voltage Protection (OVP) circuitry to disable the step-down switching regulator and LDO controller when the input voltage is above 5.7V (typical). The step-down switching regulator and LDO controller are enabled when the input voltage is below 5.6V (typical).

Figure 12: UVLO and OVP Waveforms



3.6 Thermal Shutdown

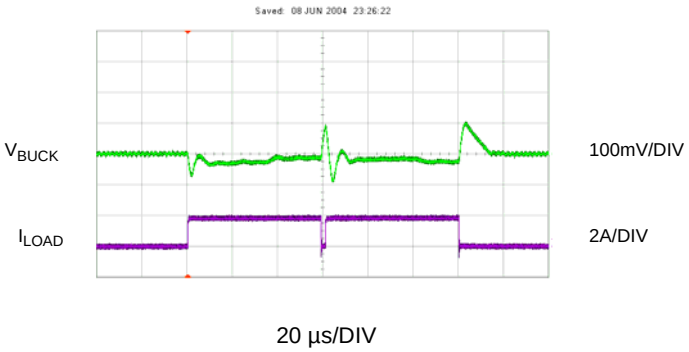
When the junction temperature of the MVPG30x/MVPG31 exceeds 150°C (typical), the thermal shutdown circuitry disables the step-down regulator. The step-down switching regulator is enabled when the junction temperature is decreased to 120°C (typical).

3.7 Adaptive Transient Response

The MVPG30x/MVPG31 device's Smart Technology allows the step-down switching regulator to quickly respond to the multiple step loads and maintain stability over a wide range of applications. Figure 13shows an example of a second step-load applied while the output voltage of the step-down switching regulator increased due to the inductive kick from the first step-load.

Condition: V_{IN} = 5.0V, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 10 µF, L = 2.0 µH, $C_{OUT(BUCK)}$ = 22 µF, I_{LOAD} = 200 mA to 2.0A.

Figure 13: Adaptive Transient Response



The overshoot (V_{SOAR}) during a full-load to light-load transient due to stored inductor energy (Figure 13) can be calculated as:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}{}^{2} \bullet L}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

Although the V_{SOAR} cannot be eliminated, its amplitude can be controlled based on the C_{OUT} capacitor value. The appropriate C_{OUT} value can easily be calculated for the acceptable V_{SOAR} level for each specific application.

$$C_{OUT} = \frac{\Delta I_{LOAD(MAX)}{}^{2} \bullet L}{2 \bullet V_{SOAR} \bullet V_{OUT}}$$

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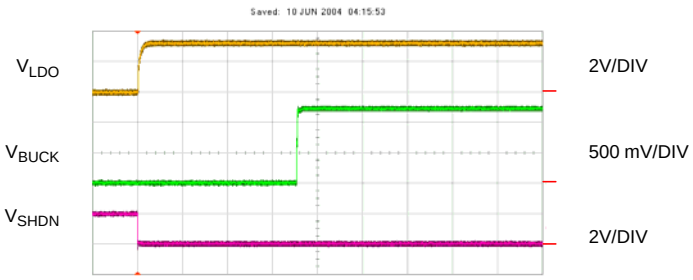
4 Functional Characteristics

The following applies unless otherwise noted: T_A = 25°C, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 10 µF, L = 2.0 µH, $C_{OUT\ (BUCK)}$ = 10 µF, PFET = FDC642P, $C_{OUT\ (LDO)}$ = 10 µF.

4.1 Startup Waveforms

NOTE: There is a delay (3.5 ms typ.) before the output voltage turns on.

Figure 14: Startup Using the Shutdown Pin

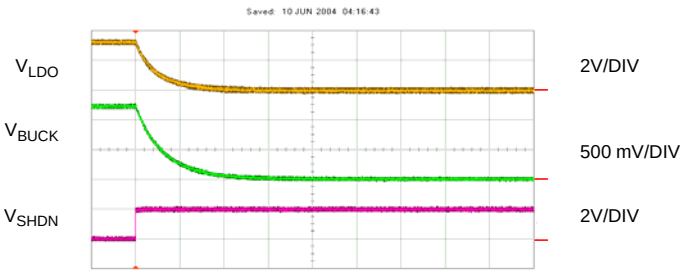


1.0 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V

I_{LOAD} = No Load
t_{DLY}~ 3.5 ms

Figure 15: Turn Off Using the Shutdown Pin

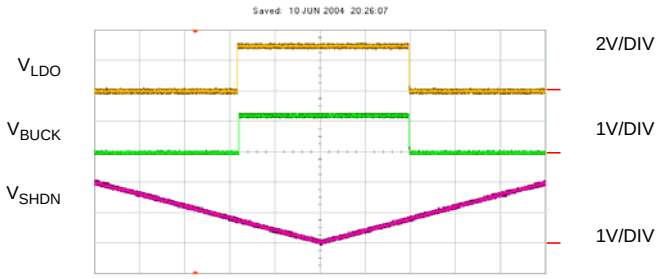


1.0 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V

I_{LOAD} = No Load

Figure 16: Enable Threshold at V_{IN} = 3.5V

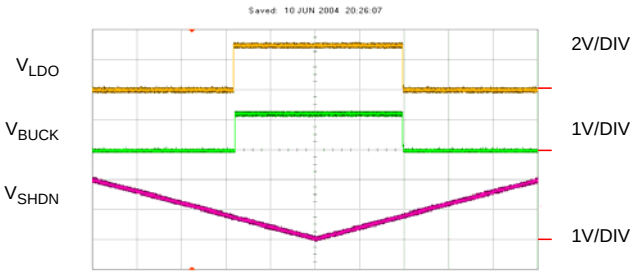


100 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V

I_{LOAD} = 10 mA
V_{TH} = 0.96V (Note)

Figure 17: Enable Threshold at V_{IN} = 5.0V

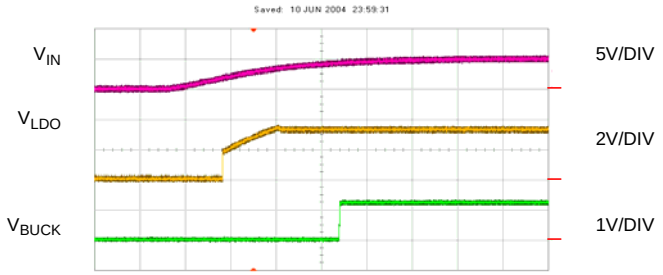


100 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V

I_{LOAD} = 10 mA
V_{TH} = 1.12V (Note)

Figure 18: Input Voltage Soft Start



2.0 ms/DIV

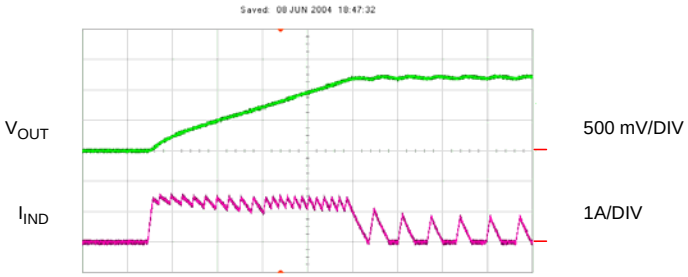
V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V
I_{LOAD} = No Load

Figure 19: Input Voltage Hot Plug

1.0 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V
I_{LOAD} = No Load

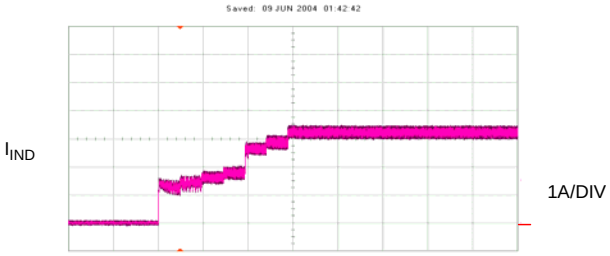
Figure 20: Step-Down Output Rise Time



5.0 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{LOAD} = 500 mA

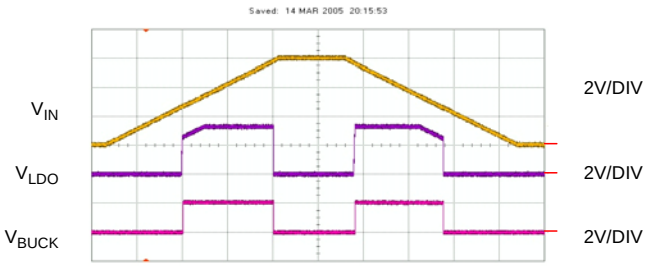
Figure 21: Soft Start Current Limit Steps



50 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 3.3V

Figure 22: UVLO and OVP Thresholds



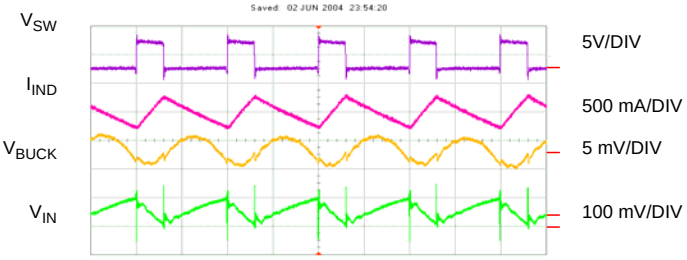
V_{IN} = 0 to 6.0V
V_{LDO} = 3.3V
V_{BUCK} = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

$V_{UVLO(HTH)}$ = 2.60V
$V_{UVLO(LTH)}$ = 2.50V
$V_{OVP(HTH)}$ = 5.8V
$V_{OVP(LTH)}$ = 5.7V

4.2 Switching Waveforms

NOTE: For repeatability of measuring output ripple ($V_{BUCK\ (P-P)}$) for the BUCK regulator, the standard test procedure limits the scope bandwidth to 20 MHz and uses a coax cable with very short leads terminated into 50Ω. The coax leads must be routed away from the switching node as much as possible.

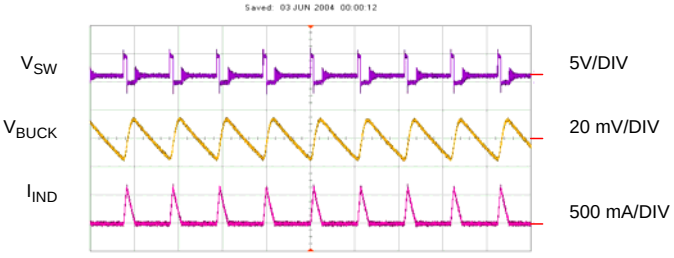
Figure 23: Switching Waveforms—PWM Mode



500 ns/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 2.0A
$V_{OUT(P-P)}$ = 6.3 mV (Note)
$V_{IN(P-P)}$ = 200.2 mV
$I_{IND(P-P)}$ = 601.5 mA
$I_{IND(PK)}$ = 2.3A
Freq = 1 MHz

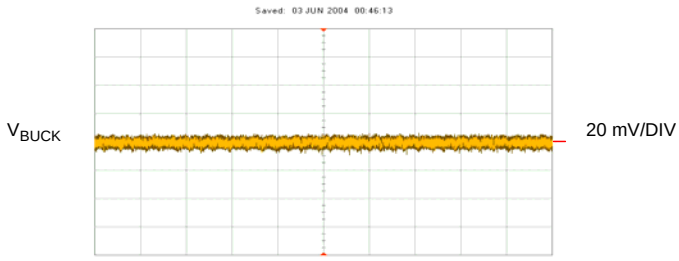
Figure 24: Switching Waveforms—DCM Mode



5.0 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 50 mA
$V_{OUT(P-P)}$ = 31.4 mV (Note)
$I_{IND(PK)}$ = 670.4 mA
Freq = 185 kHz

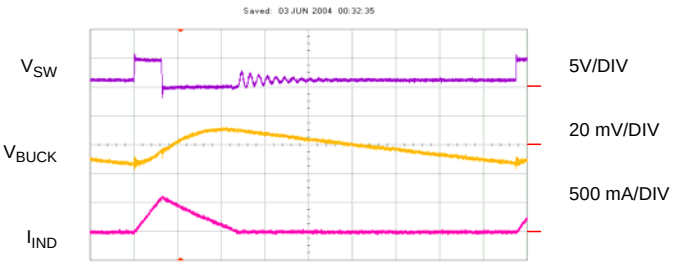
Figure 25: PWM Output Ripple Voltage



100 ms/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 2.0A
$V_{OUT(P-P)}$ = 15.7 mV (Note)

Figure 26: Switching Waveforms—DCM Mode-Zoom



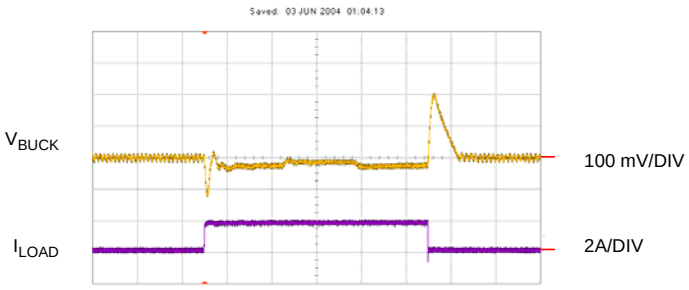
500 ns/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 50 mA
Ringing Freq = 10 MHz

4.3 Load Transient Waveforms

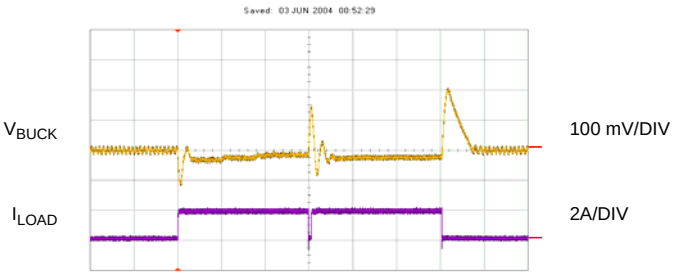
4.3.1 Step-Down Regulator

Figure 27: Load Transient Response



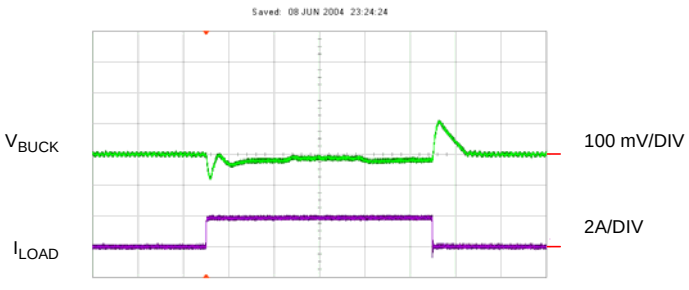
V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 22 µF
I_{LOAD} = 200 mA to 2.0A
t_{RISE} = 6.0A/µs
t_{FALL} = 129A/µs

Figure 28: Double-Pulsed Load Response



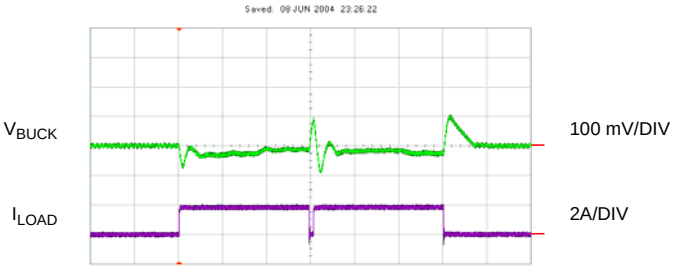
V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 22 µF
I_{LOAD} = 200 mA to 2.0A
t_{RISE} = 6.0A/µs
t_{FALL} = 129A/µs

Figure 29: Load Transient Response



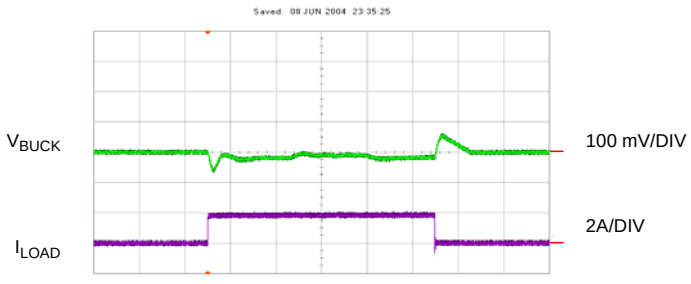
V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 2x22 µF
I_{OUT} = 200 mA to 2.0A
t_{RISE} = 6.0A/µs
t_{FALL} = 129A/µs

Figure 30: Double-Pulsed Load Response



V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 2x22 µF
I_{OUT} = 200 mA to 2.0A
t_{RISE} = 6.0A/µs
t_{FALL} = 129A/µs

Figure 31: Load Transient Response



V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 4x22 µF
I_{LOAD} = 200 mA to 2.0A
t_{RISE} = 6.0A/µs
t_{FALL} = 129A/µs

Figure 32: Double-Pulsed Load Response

V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 4x22 µF
I_{LOAD} = 200 mA to 2.0A
t_{RISE} = 6.0A/µs
t_{FALL} = 129A/µs

4.3.2 LDO Regulator

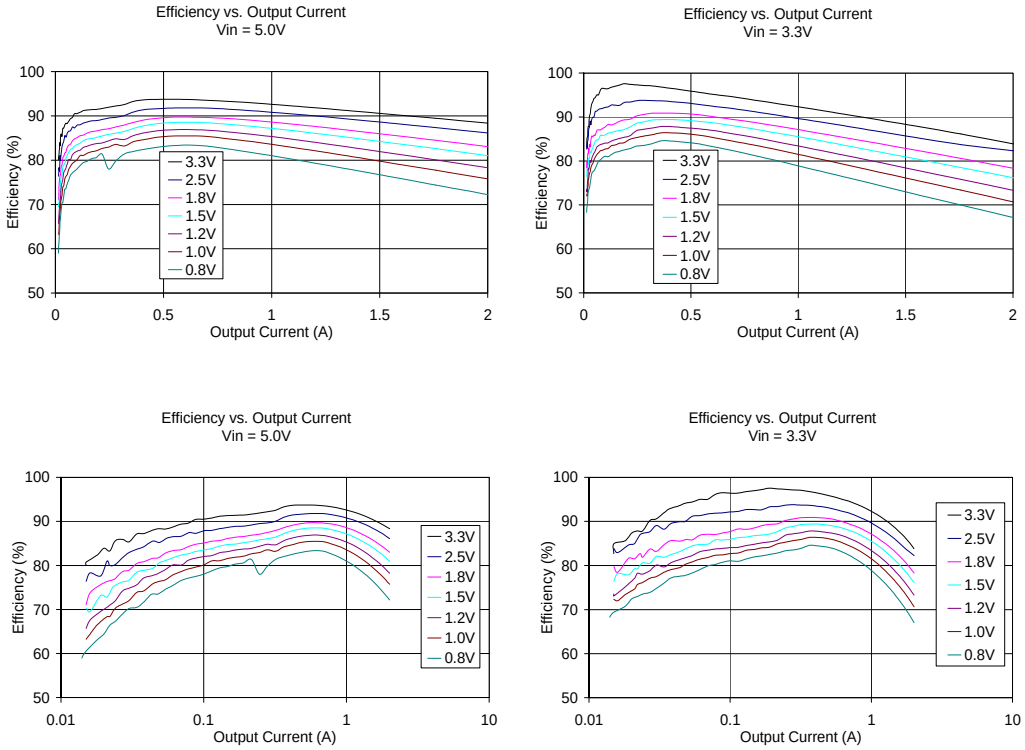
Figure 33: Load Transient Response

V_{IN} = 5.0V
V_{LDO}= 3.3V
C_{OUT} = 10 µF
I_{LOAD} = 0.2A to 0.8 mA

5 Typical Characteristics

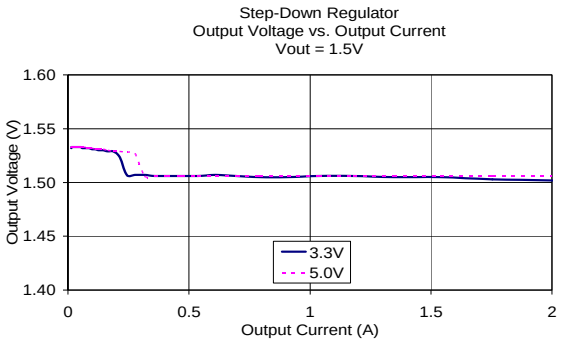
5.1 Efficiency Graphs

Figure 34: Efficiency Graphs



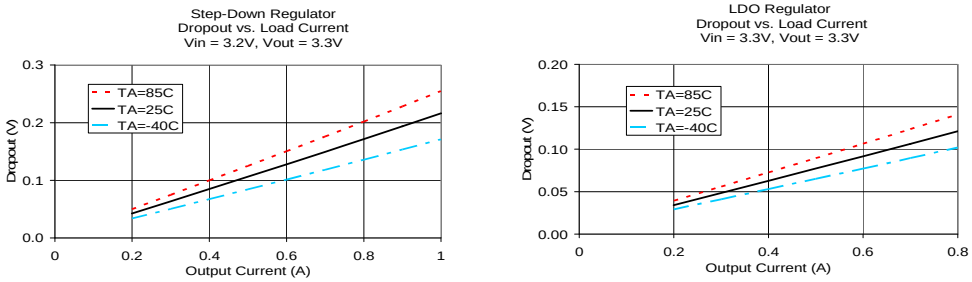
5.2 Load Regulation

Figure 35: Load Regulation



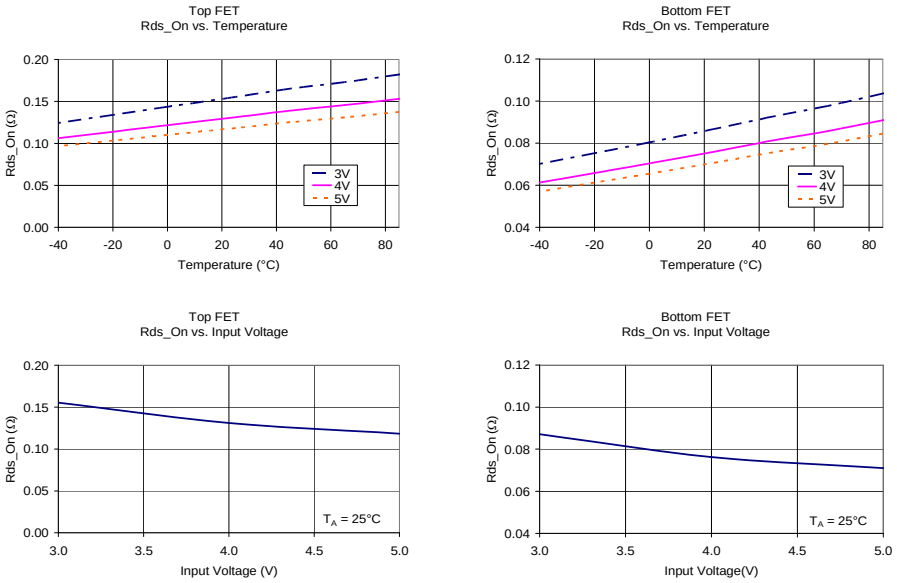
5.3 Dropout Voltage

Figure 36: Dropout Voltage



5.4 RDS (ON) Resistance

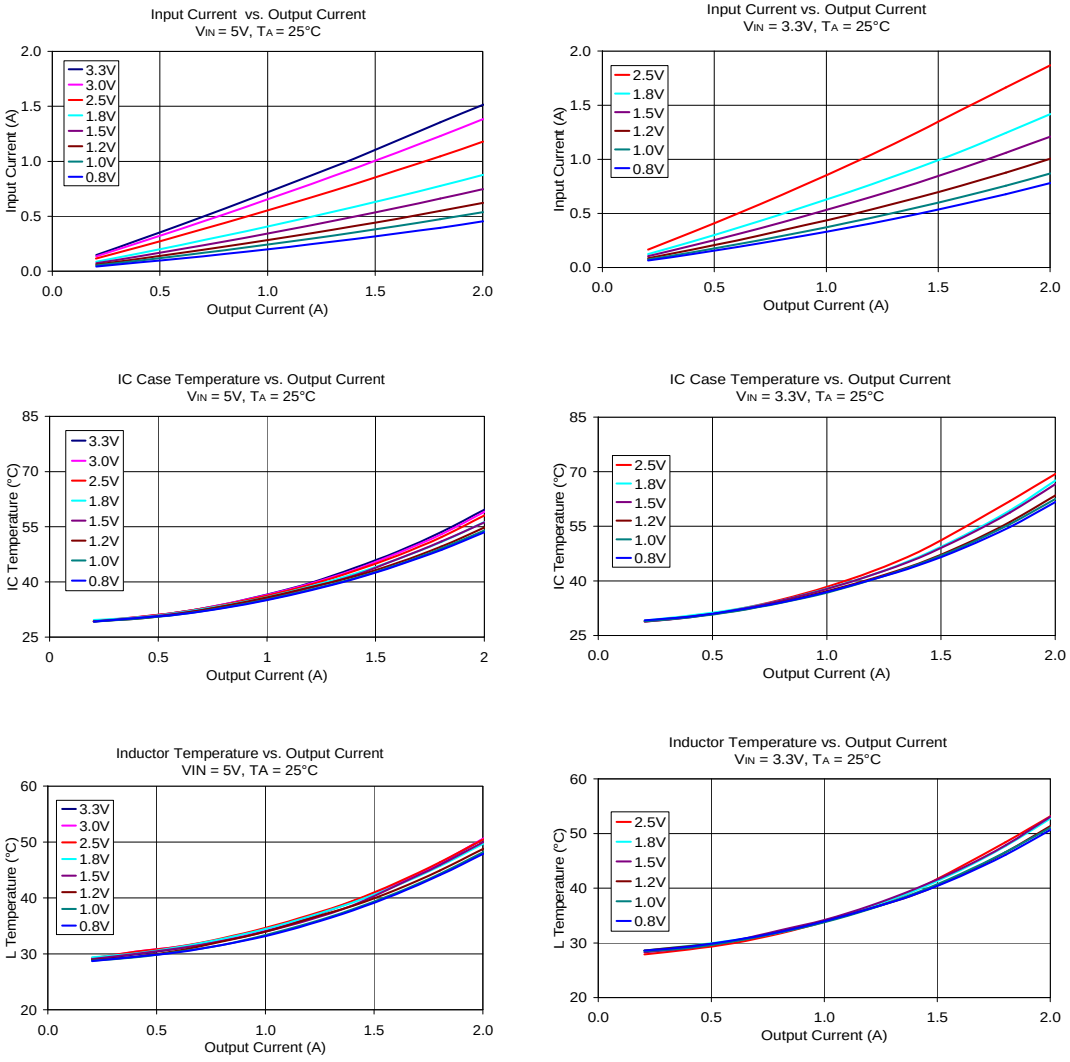
Figure 37: RDS (ON) Resistance



5.5 IC Case and Inductor Temperature

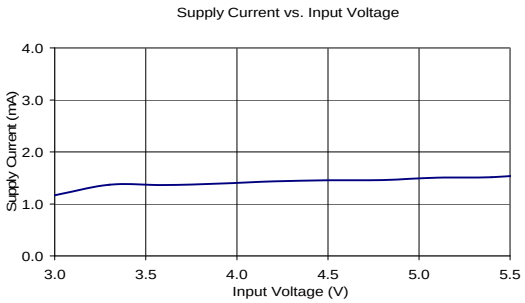
The following data was taken using a 0.625 square inch and L = 2.0 µH. Actual results depend upon the size of the PCB proximity to other heat emitting components.

Figure 38: IC Case and Inductor Temperature



5.6 Input Voltage Graph

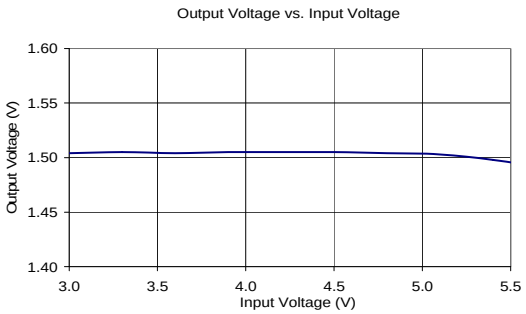
Figure 39: Supply Current vs. Input Voltage



Load = No Load

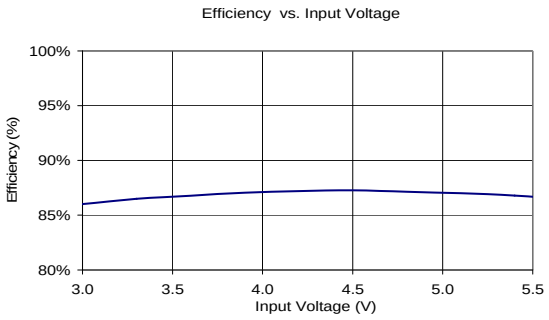
5.6.1 Step-Down Regulator

Figure 40: Output Voltage vs. Input Voltage



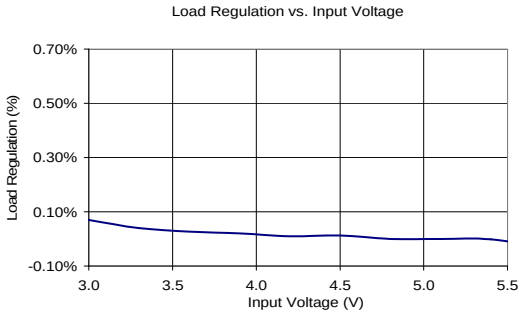
$I_{OUT(BUCK)}$ = 500 mA

Figure 41: Efficiency vs. Input Voltage



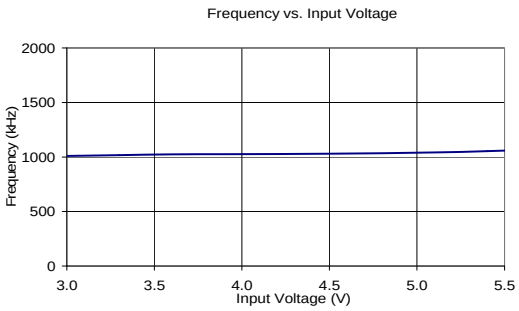
V_{IN} = 5.0V
$V_{OUT(BUCK)}$ = 1.5V
$I_{OUT(BUCK)}$ = 1.0A

Figure 42: Load Regulation vs. Input Voltage



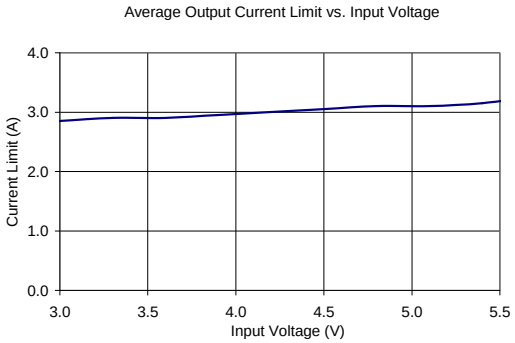
V_{IN} = 5.0V
$V_{OUT(BUCK)}$ = 1.5V
$I_{OUT(BUCK)}$ = 500 mA to 2.0A

Figure 43: Frequency vs. Input Voltage



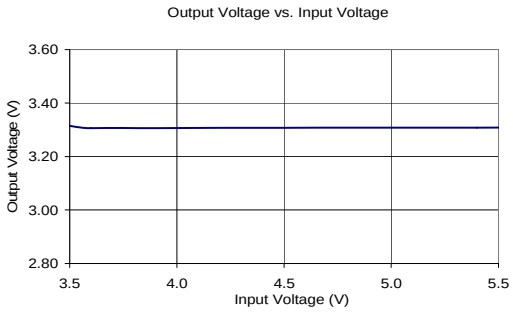
$I_{OUT(BUCK)}$ = 1.0A

Figure 44: Average Output Current Limit vs. Input Voltage



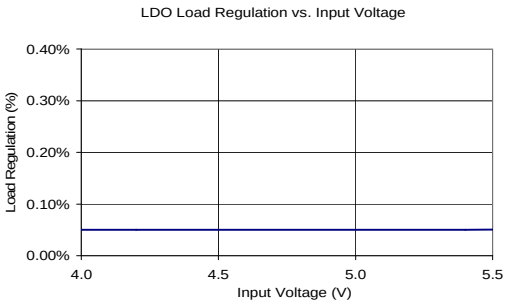
5.6.2 LDO Regulator

Figure 45: Output Voltage vs. Input Voltage



$I_{OUT(LDO)}$ = 10 mA

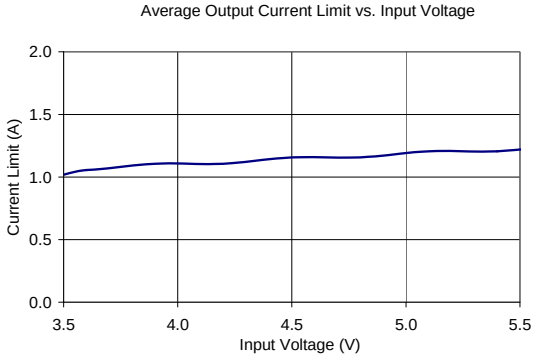
Figure 46: LDO Load Regulation vs. Input Voltage



$V_{OUT(LDO)}$ = 3.3V

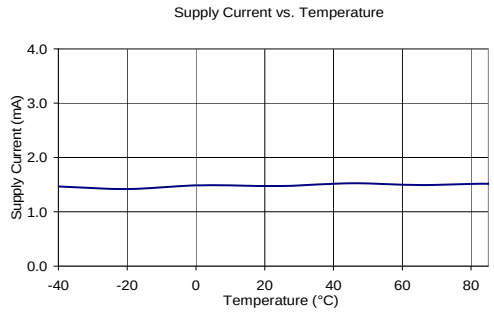
$I_{OUT(LDO)}$ = 10 mA to 800 mA

Figure 47: Average Output Current Limit vs. Input Voltage



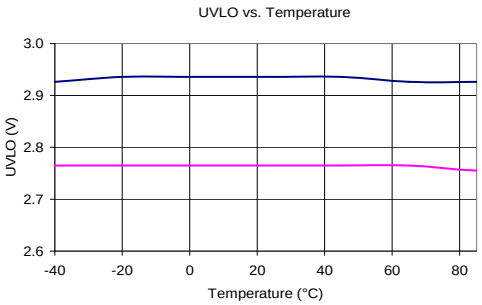
5.7 Temperature Graphs

Figure 48: Supply Current vs. Temperature



$I_{OUT(BUCK)}$ = No Load $I_{OUT(LDO)}$ = No Load

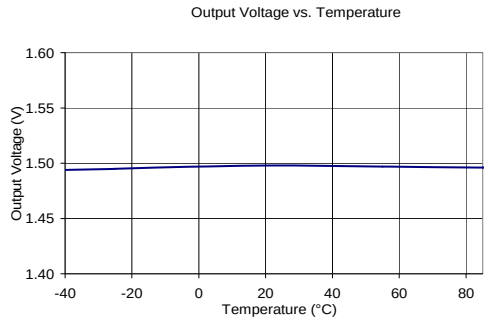
Figure 49: UVLO vs. Temperature



$I_{OUT(BUCK)}$ = 10 mA

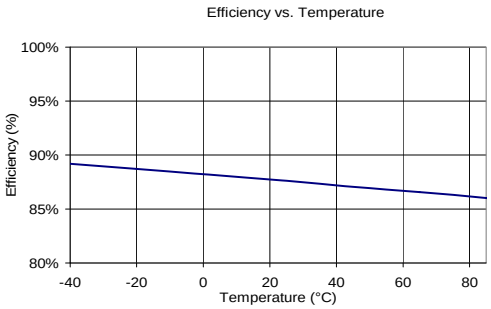
5.7.1 Step-Down Regulator

Figure 50: Output Voltage vs. Temperature



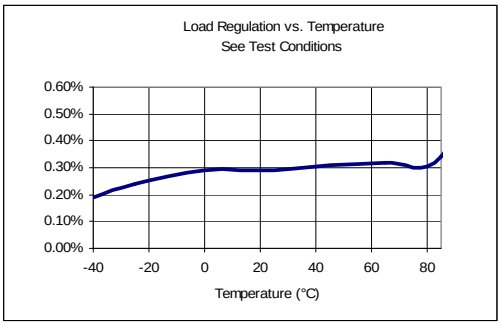
V_{IN} = 5.0V $I_{OUT(BUCK)}$ = 500 mA

Figure 51: Efficiency vs. Temperature



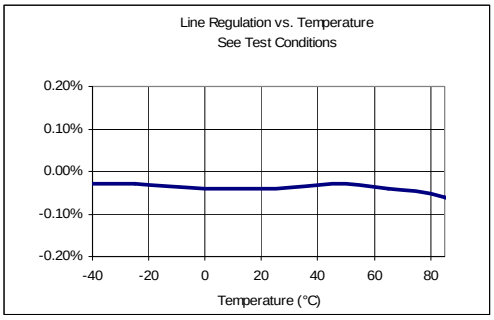
V_{IN} = 5.0V $I_{OUT(BUCK)}$ = 1.0A
$V_{OUT(BUCK)}$ = 1.5V

Figure 52: Load Regulation vs. Temperature



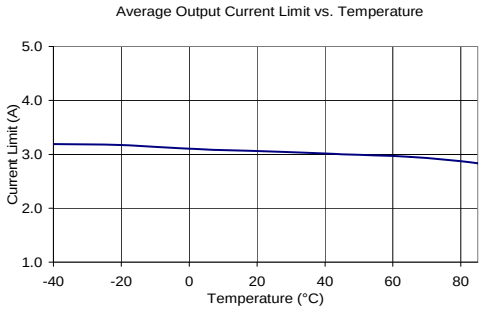
V_{IN} = 5.0V
$V_{OUT(BUCK)}$ = 1.5V
$I_{OUT(BUCK)}$ = 500 mA to 2.0A

Figure 53: Line Regulation vs. Temperature



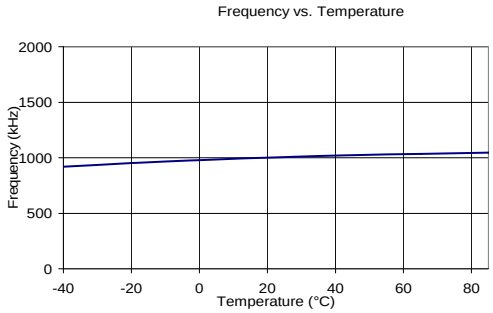
V_{IN} = 3.0V to 5.0V
$V_{OUT(BUCK)}$ = 1.5V
$I_{OUT(BUCK)}$ = 500 mA

Figure 54: Average Output Current Limit vs. Temperature



V_{IN} = 5.0V

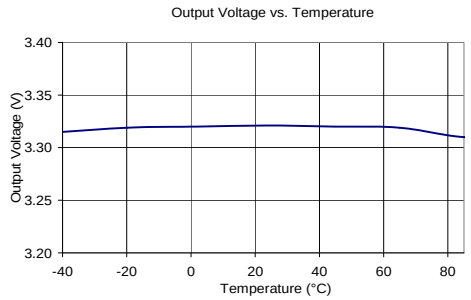
Figure 55: Frequency vs. Temperature



V_{IN} = 5.0V
$V_{OUT(BUCK)}$ = 1.5V
$I_{OUT(BUCK)}$ = 1.0A

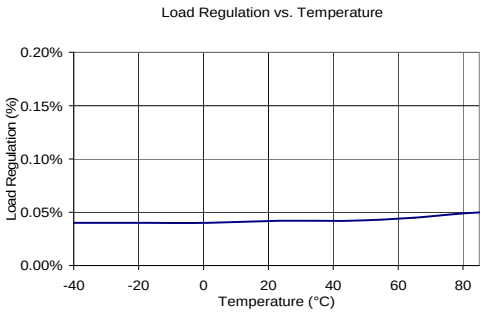
5.7.2 LDO Regulator

Figure 56: Output Voltage vs. Temperature



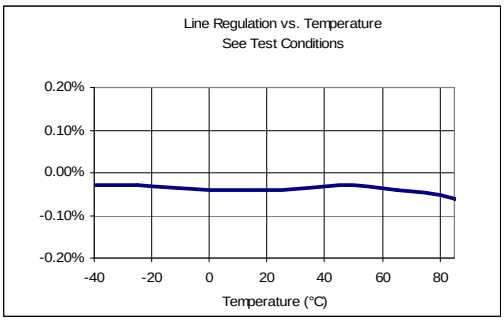
V_{IN} = 5.0V $I_{OUT(LDO)}$ = 10 mA

Figure 57: Load Regulation vs. Temperature



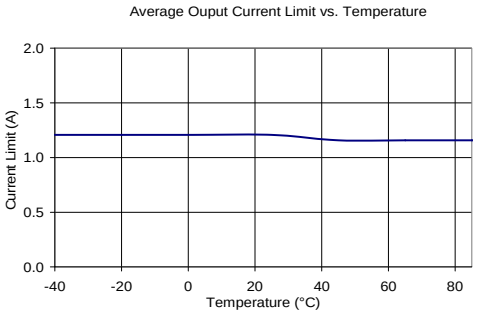
V_{IN} = 5.0V $I_{OUT(LDO)}$ = 10 mA to 800 mA
$V_{OUT(LDO)}$ = 3.3V

Figure 58: Line Regulation vs. Temperature



V_{IN} = 3.5V to 5.0V $I_{OUT(LDO)}$ = 10 mA
$V_{OUT(LDO)}$ = 3.3V

Figure 59: Average Output Current Limit vs. Temperature



V_{IN} = 5.0V

6 Applications Information

6.1 PC Board Layout Considerations and Guidelines

Warning To avoid noise and abnormal operating behavior, follow these layout recommendations.

1. This is a 2-layer board with one ground plane and one routing layer.
2. Copy the routing layer in Figure 64 or Figure 65 as much as possible and place it on the top layer. The ground plane in Figure 66 or Figure 67 can be placed on any other layer. Use the recommend BOM in Table 11 or Table 12. Contact the factory where substitutions are made.
3. Review the recommended solder pad layout and notes in Section 7.3, Typical Pad Layout Dimensions, on page 59.
4. Do not replace the Ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor in placed next to the IC. If Tantalum input capacitor is used, it must be rated for switching regulator applications and the operating voltage be derated by 50%.
5. Use either X7R or X5R type ceramic capacitors. If Y5V or Z5U type capacitor are used, then you must double the recommended capacitance value.
6. Any type of capacitor can be placed in parallel with the output capacitor.
7. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that the Ceramic capacitors provide the lowest noise and smallest foot print solution.
8. Use planes for the ground, input and outputs power to maintain good voltage filtering and to keep power losses low.
9. If there is not enough space for a power plane for the input supply, then the input supply trace must be at least 3/8 inch wide.
10. If there is not enough space for a power plane for the output supplies, then place the output as close to the load as possible with a trace of at least 3/8 inch wide.
11. Do not lay out the inductor first. The input capacitor placement is the most critical for proper operation. The AC current circulating through the input capacitor and loop 1 (LP1) are square wave with rise and fall times of 8 ns and slew rates as high as 300 A/µs (see Figure 60). At these fast slew rates, stray PCB inductance can generate a voltage spike as high as 3.0V per inch of PCB trace, VIND = L * di/dt. Therefore, the Ceramic input capacitor must be place as close as possible to the PVIN and PGND pins with as short and wide trace as possible. Also, the PVIN and PGND traces must be placed on the top layer. This will isolate the fast AC currents from interfering with the analog ground plane.
12. The MVPG30x/MVPG31 has two internal grounds, analog (SGND) and power (PGND). The analog ground ties to all the noise sensitive signals (PSET, VSET, and SVIN) while the power ground ties to the higher current power paths. Noise on an analog ground can cause problems with the IC's internal control and bias signals. For this reason, separate analog and power ground traces are recommended. The signal ground is connected to the power ground at one point, which is the (-) terminal of the output capacitor.

13. Keep loop 2 (LP2) as small as possible and connect the (-) terminal of the output capacitor as close to the (-) terminal of the input capacitor. A back-to-back placing of bypass capacitors, as shown in Figure 60 or Figure 61, is recommended for best results.
14. Keep the switching node (SW) away from the SFB pin and all sensitive signal nodes, minimizing capacitive coupling effects. If the SFB trace must cross the SW node, cross it at a right angle.
15. Try not to route analog or digital lines in close proximity to the power supply especially the VSW node. If this can't be avoided, shield these lines with a power plane placed between the VSW node and the signal lines.
16. The type of solder paste recommended for QFN packages is "No clean", due to the difficulty of cleaning flux residues from beneath the QFN package.

Figure 60: MVPG30x PCB Layout Schematic

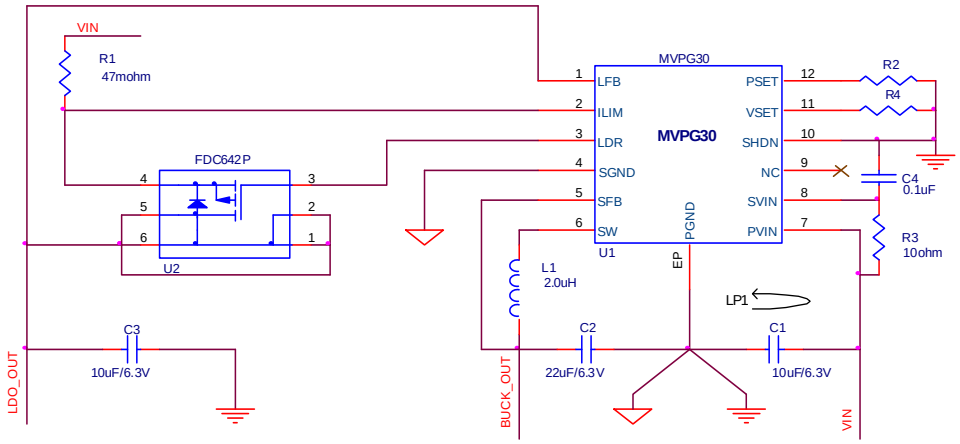
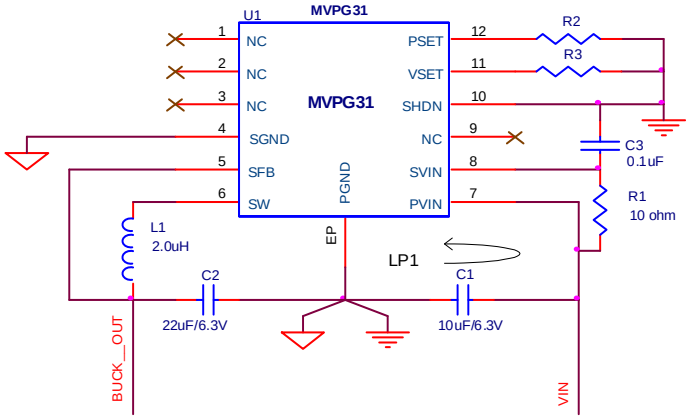


Figure 61: MVPG31 PCB Layout Schematic



6.1.1 PC Board Layout Examples for MVPG30x/MVPG31

For the MVPG30x:

- Actual board size = 565 mil x 945 mil; Area = 0.534 Sq. Inches.
- Total copper layers = 2 (Top and Bottom)
- All the components are on the top layer

For the MVPG31:

- Actual board size = 420 mil x 725 mil; Area = 0.305 Sq. Inches.
- Total copper layers = 2 (Top and Bottom)
- All the components are on the top layer

Figure 62: Top Silk-Screen (Not to scale)—MVPG30x

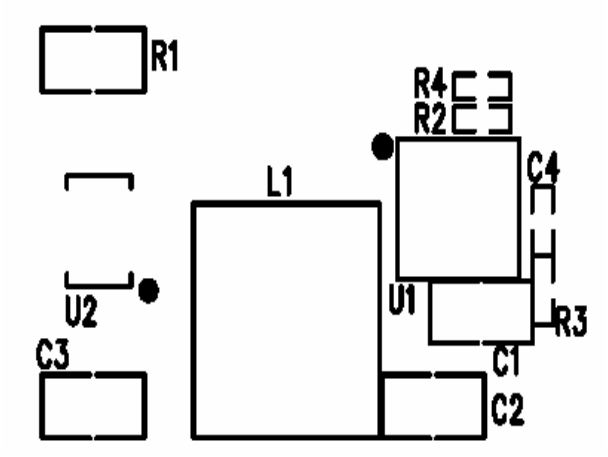


Figure 63: Top Silk-Screen (Not to scale)—MVPG31

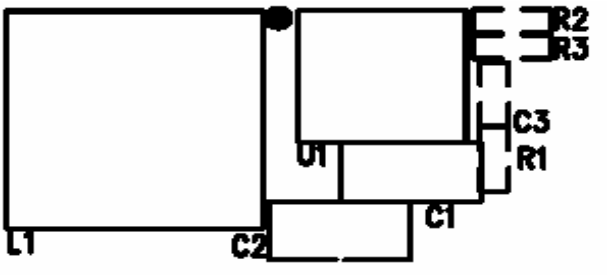


Figure 64: Top Traces, Vias, and Copper (Not to scale)—MVPG30x

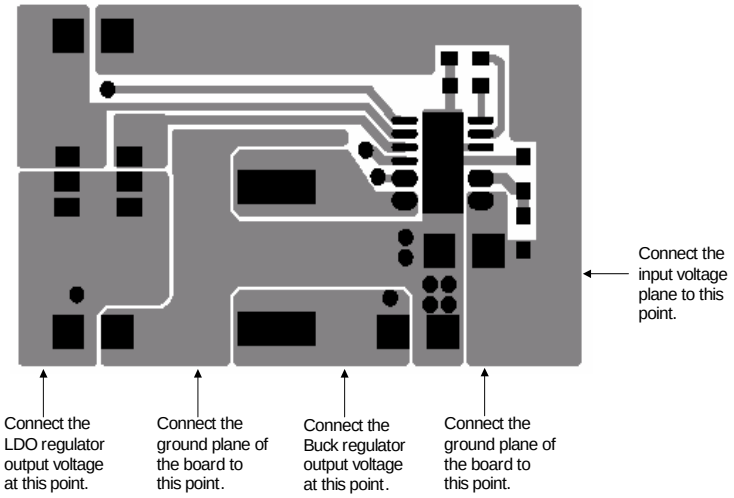


Figure 65: Top Traces, Vias, and Copper (Not to scale)—MVPG31

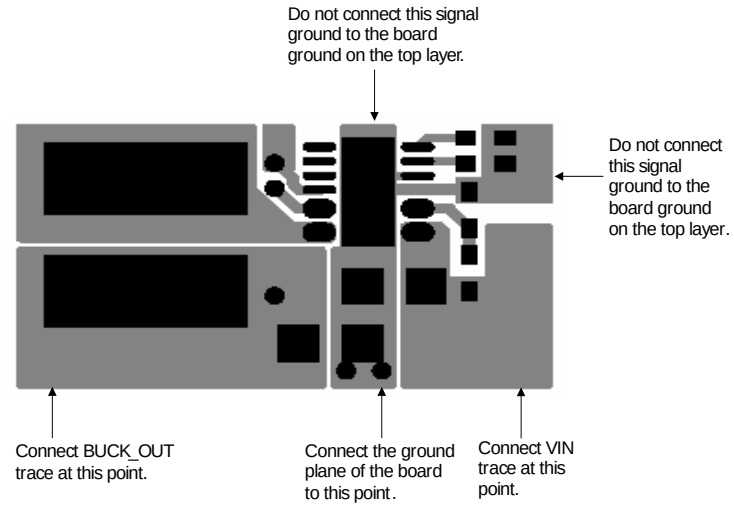


Figure 66: Bottom Silk Screen, Bottom Trace, Vias, and Bottom Copper (Not to scale)—MVPG30x

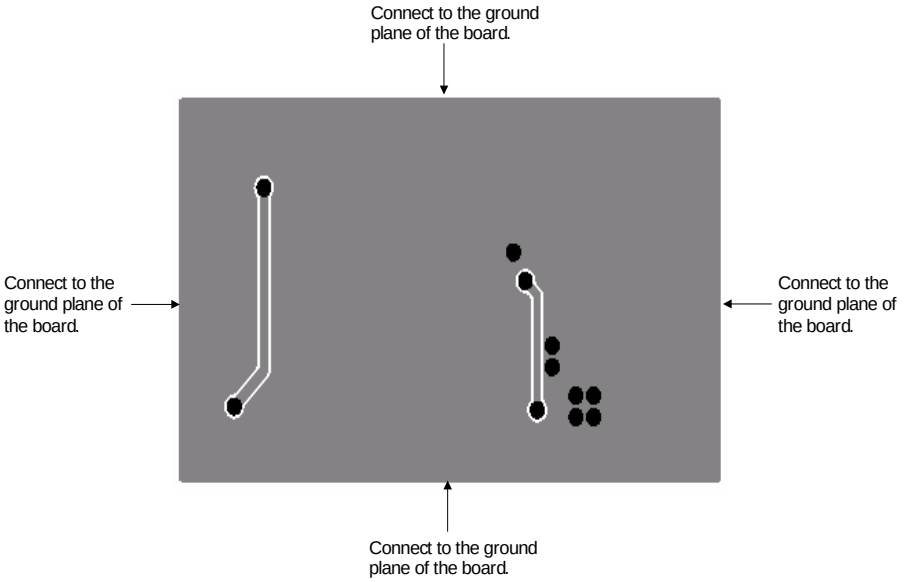
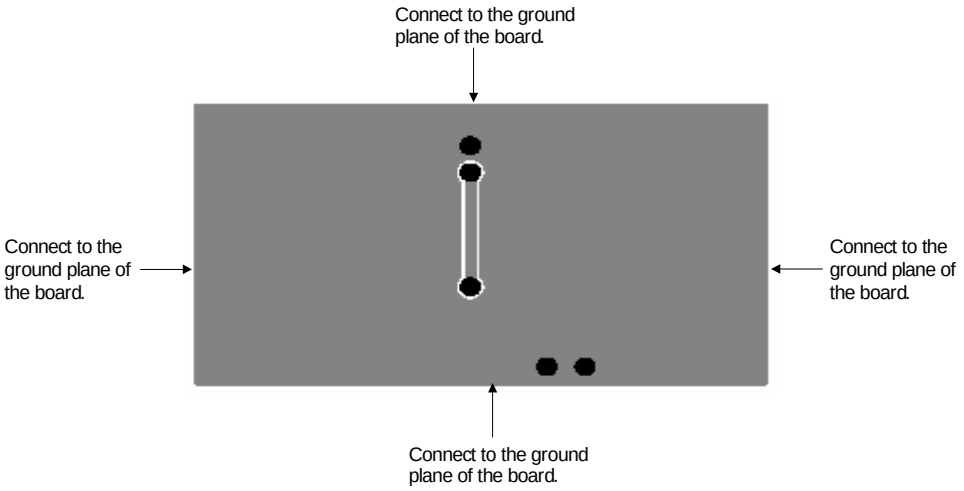


Figure 67: Bottom Silk Screen, Bottom Trace, Vias, and Bottom Copper (Not to scale)—MVPG31



6.2 Bill of Materials

The following tables list the components used with the MVPG30x/MVPG31.

Table 11: MVPG30x BOM

Item	Qty	Ref	Manufacturer Part No.	Manufacturer	Description
1	**1**	**U1**	**MVPG30B**	**Marvell Semiconductor**	**1 MHz, 3.0A Peak Current-Limit Step-Down Regulator with LDO regulator controller**
2	1	U2	FDC642P	Fairchild	P-FET, 2.5V, SuperSOT-6 package
3	1	C1	CE JMK212 BJ106MG-T	Taiyo-Yuden	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
4			C2012X5R0J106MT	TDK	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	1	C2	CE JMK212 BJ226MG-T	Taiyo-Yuden	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
6			C2012X5R0J226MT	TDK	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
7	1	C3	CE JMK212 BJ106MG-T	Taiyo-Yuden	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
8			C2012X5R0J106MT	TDK	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
9	1	C4	RM LMK105 BJ104KV-F	Taiyo-Yuden	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
10			C1005X5R1A104K	TDK	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
11	1	L1	A918CY-2R0M=P3	Toko	2.0 µH, 2.47A (typ.), 24 mΩ (typ.), H = 2mm, L = 6.2 mm, W = 6.3 mm
12	1	R1	RL1220T-R047-J	Susumu Co. Ltd.	0.047Ω, 1/4W, 5%, 0805 Case Size
13	1	R2			See Section 3.2, Output Voltage—AnyVoltage™ Technology, on page 26.
14	1	R3	ERJ-2RKF10R0X	Panasonic-ECG	10Ω, 1/16W, 1%, 0402 Case Size
15	1	R4			See Section 3.2, Output Voltage—AnyVoltage™ Technology, on page 26.

Table 12: MVPG31 BOM

Item	Qty	Ref	Manufacturer Part No.	Manufacturer	Description
1	**1**	**U1**	**MVPG31**	**Marvell Semiconductor**	**1 MHz, 3.0A Peak Current-Limit Step-Down Regulator**
2	1	C1	CE JMK212 BJ106MG-T	Taiyo-Yuden	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
3			C2012X5R0J106MT	TDK	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
4	1	C2	CE JMK212BJ226MG-T	Taiyo-Yuden	22 µF ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5			C2012X5R0J226MT	TDK	22 µF ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
6	1	C4	RM LMK105 BJ104KV-F	Taiyo-Yuden	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
7			C1005X5R1A104K	TDK	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
8	1	L1	A918CY-2R0M=P3	Toko	2.0 µH, 2.47A (typ.), 24 mΩ (typ.), H = 2mm, L = 6.2 mm, W = 6.3 mm
9	1	R1	ERJ-2RKF10R0X	Panasonic-ECG	10Ω, 1/16W, 1%, 0402 Case Size
10	1	R2			See Section 3.2, Output Voltage—AnyVoltage™ Technology, on page 26
11	1	R3			See Section 3.2, Output Voltage—AnyVoltage™ Technology, on page 26

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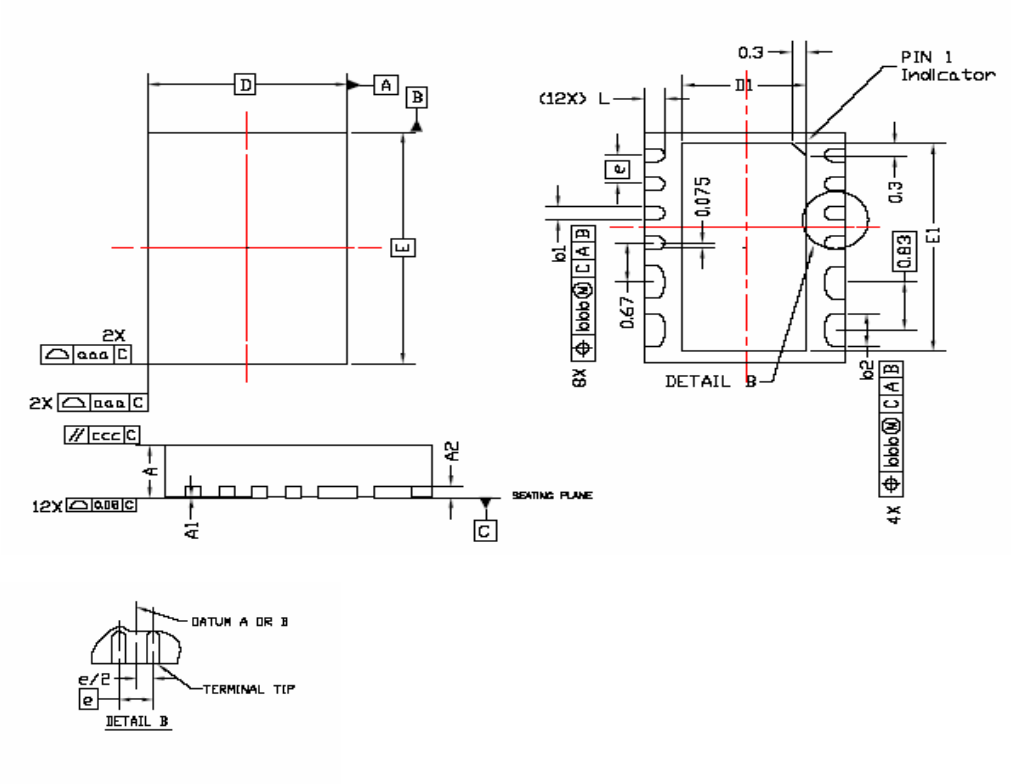
7 Mechanical Drawing

7.1 Mechanical Drawing

Figure 68: Mechanical Drawing



7.2 Dimensions

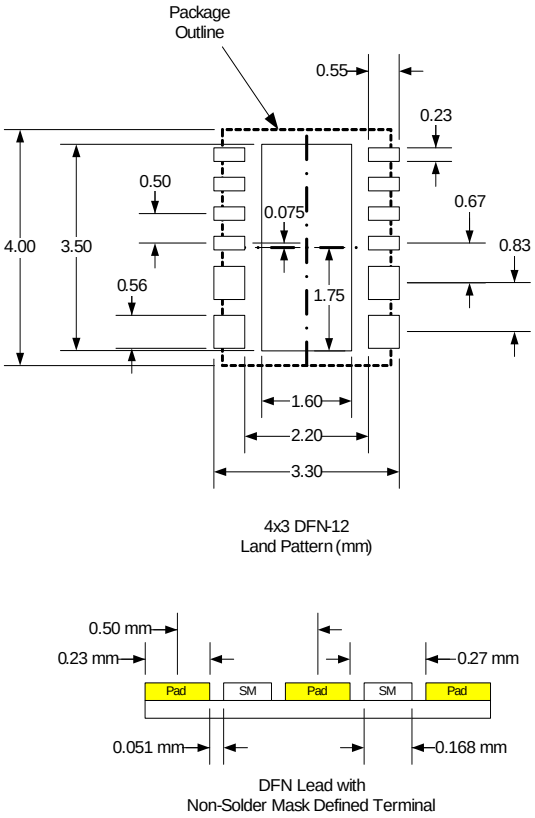
Table 13: Dimensions

Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2		0.20 REF			0.008 REF	
b1	0.18	0.23	0.28	0.007	0.009	0.011
b2	0.51	0.56	0.61	0.020	0.022	0.024
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	1.60	1.70	1.80	0.063	0.067	0.071
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	3.40	3.50	3.60	0.134	0.138	0.142
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
aaa	--	--	0.15	--	--	0.006
bbb	--	--	0.10	--	--	0.004
ccc	--	--	0.10	--	--	0.004

7.3 Typical Pad Layout Dimensions

7.3.1 Recommended Solder Pad Layout

Figure 69: Recommended Solder Pad Layout



Note

- Top view
- Drawing not to scale
- Dimensions are in millimeters
- Exposed pad shall be copper plated
- Oversize solder mask by 0.102 mm (4 mils) over pad size (0.051 mm annular ring)
- 0.168 mm solder mask (sm) between pads
- Tolerance ±0.05 mm

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8 Part Order Numbering/Package Marking

8.1 Part Order Numbering

Figure 70 shows the part order numbering scheme for the MVPG30x/MVPG31. Refer to Marvell Field Applications Engineers (FAEs) or representatives for further information when ordering parts.

Figure 70: Sample Part Order Number

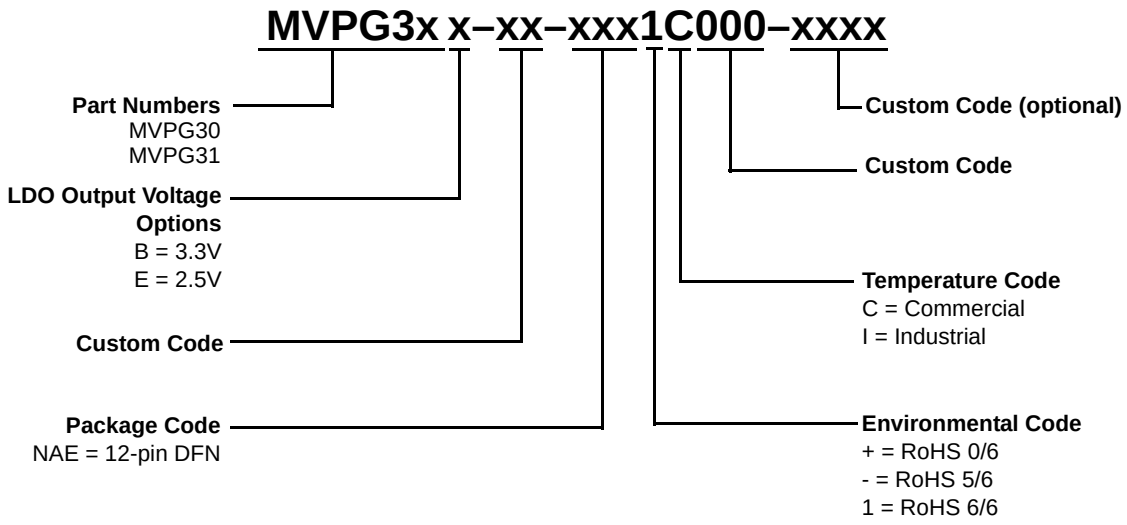


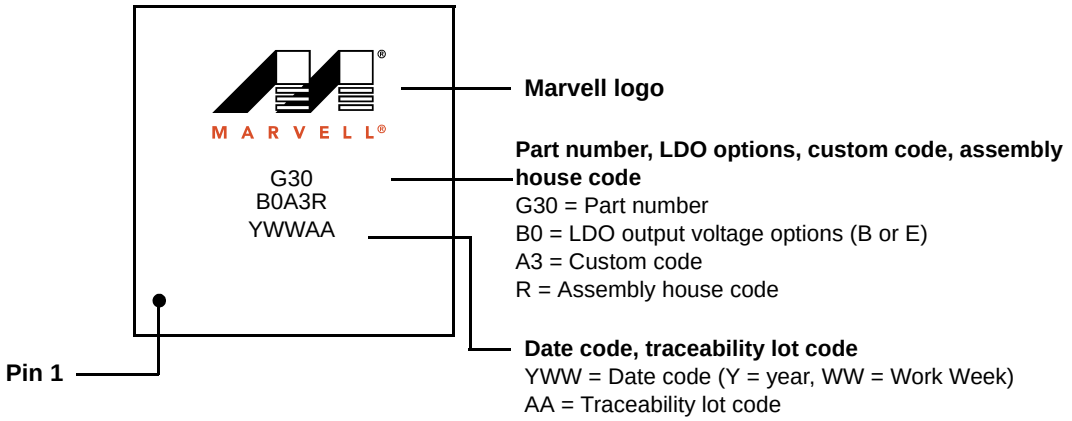
Table 14: Part Order Options

Package Type	Marking	LDO	Ambient Temperature Range	Part Order Number
4 mm x 3 mm 12-pin DFN	B0	3.3V	-40°C to 85°C	MVPG30B-xx-NAE1C000
4 mm x 3 mm 12-pin DFN	E0	2.5V	-40°C to 85°C	MVPG30E-xx-NAE1C000
4 mm x 3 mm 12-pin DFN	00	--	-40°C to 85°C	MVPG31-xx-NAE1C000

8.2 Package Marking

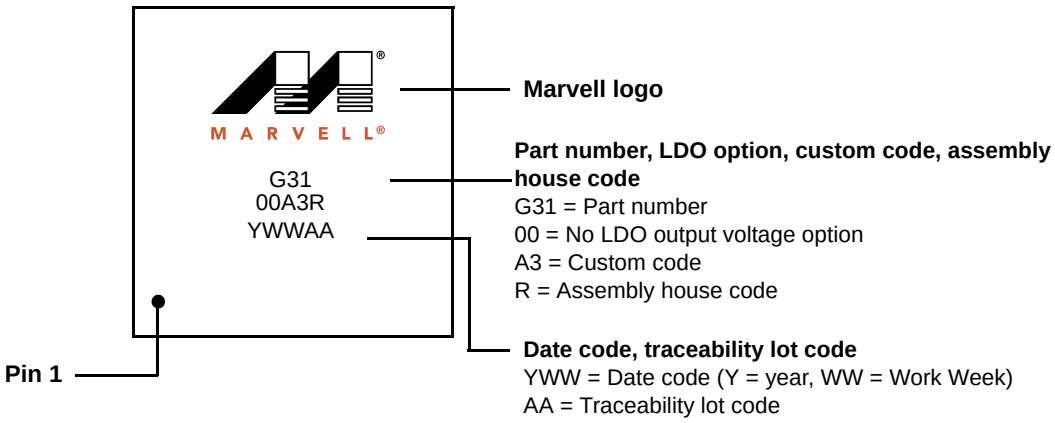
This section show the sample package markings and pin 1 location.

Figure 71: MVPG30x Package Marking



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 72: MVPG31 Package Marking



Note: The above drawing is not drawn to scale. Location of markings is approximate.

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A Revision History

Table 15: Revision History

Document Type	Document Revision
Release	Rev.G
Electrical Specifications Updated V_{UVLO} values in Table 5, Electrical Characteristics, on page 19	

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